A 3-D PWM CONTROL, H-BRIDGE TRI-LEVEL INVERTER FOR POWER QUALITY COMPENSATION IN THREE-PHASE FOUR-WIRED SYSTEMS

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ABSTRACT

A three-dimensional pulse width modulation (3-D PWM) control, H-bridge tri-level inverter, acts as a power quality compensator for three-phase four-wired systems, is proposed. Such compensator is an alternative of diode-clamped inverter based one, which generally suffers from the DC-link voltage unbalance problem and possesses low expandability in very high-voltage and high-power applications. This paper based on the concepts of switching function and state-variable formulation to deduce the mathematical model of H-bridge tri-level inverter, with also an enhanced switching table that balances the average switching frequency of the switches. The compensation is accomplished through a sign cubical hysteresis control strategy, which controls the total 27 space vectors in 3-D aspect to inject the nearest negative amplitude of harmonics into the load currents to compensate both the harmonic and in-phase currents into the systems to reduce the peak-load power supply from the generator. System-level simulation results demonstrate the feasibility and performance of such compensator.

1. INTRODUCTION

In power distribution networks, both three-phase three-wired and three-phase four-wired systems are particularly important. Due to the non-linear loading effects, the power quality of the neighbor systems will be degraded significantly. In order to minimize such disturbance, a power quality compensator (or an active filter), typically constructed by multilevel inverter, can be adopted. In the literature, different kinds and different levels inverter have been proposed for three-phase three-wired systems with two-dimensional pulse width modulation (2-D PWM) control [1]-[4]. There are seldom papers that focus on three-phase four-wired systems, in which the extra neutral line makes the traditional 2-D PWM not applicable. Recently, 3-D PWM has been proposed and demonstrated in a diode-clamped tri-level inverter [Fig. 1(a)] for power quality compensation, motor drivers or peak-load power supply [5]-[7]. The space vectors are considered in 3-D aspect to take consider both the three-phase power lines as well as the neutral one without the need of four arms-inverter. However, the diode-clamped inverter suffers from the natural problems of DC-link voltage unbalance, and the difficulty to alter the number of clamping diode as the voltage level changes, thus it is very inefficient in expansion to higher-level architecture based on low-level one.

In this paper, a 3-D PWM control, tri-level H-bridge inverter [8] as shown in Fig. 1(b) is proposed in order to attain the highest expandability for higher-voltage and higher-power applications, since the level of the inverter is proportional with the number of H-bridge cell that cascaded together. The disadvantage is obviously the increased number of DC sources, but it is still worth to make such choice in considering the global manufactory costs.

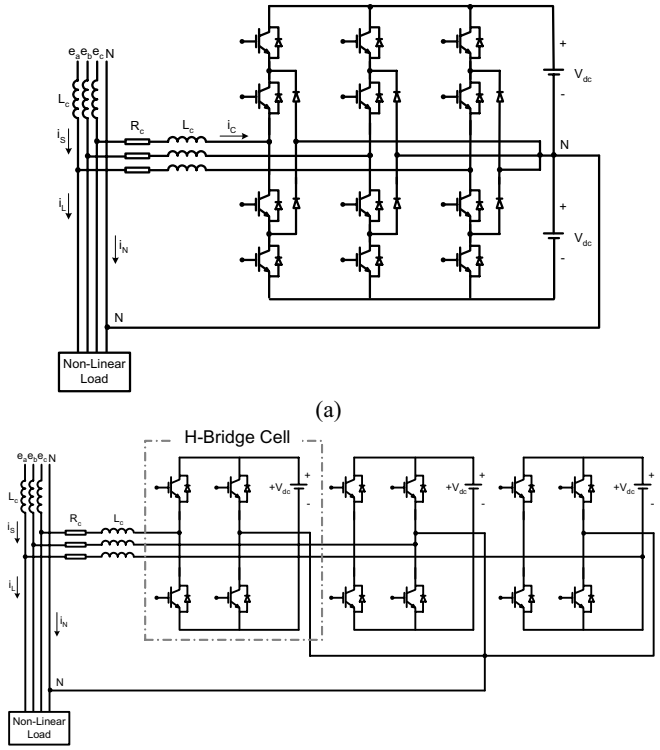


Fig. 1. Tri-level inverter as power quality compensator for three-phase four-wired systems. (a) Diode-clamped, and (b) H-bridge.

2. H-BRIDGE TRI-LEVEL INVERTER AND ITS MATHEMATICAL MODEL

This section analyzes the structure of an H-bridge tri-level inverter as a power quality compensator. The basic principle is to inject the same negative amplitude of harmonics into the load current in order to compensate the harmonic current and the in-phase current into the systems to reduce the peak-load power supply from the generator. The losses of the switching devices and snubber circuits, and process of commutation are ignored so that the equivalent switched-circuit can be obtained as shown in Fig. 2.

The model of H-bridge three-phase four-wired tri-level inverter is investigated in the *a-b-c* frame. Switching functions can be considered as the equivalent switched devices such as IGBT's, e.g., in phase **A**, S_a may be written as:

$$S_a = \begin{cases} 1, & when \;\; S_{a2} \,\&\, S_{a3} \;\; are \;\; closed \\ 0, & when \;\; S_{a1} \,\&\, S_{a2} \;\; or \;\; S_{a3} \,\&\, S_{a4} \;\; are \;\; closed \\ -1, & when \;\; S_{a1} \,\&\, S_{a4} \;\; are \;\; closed \end{cases} \quad (1)$$

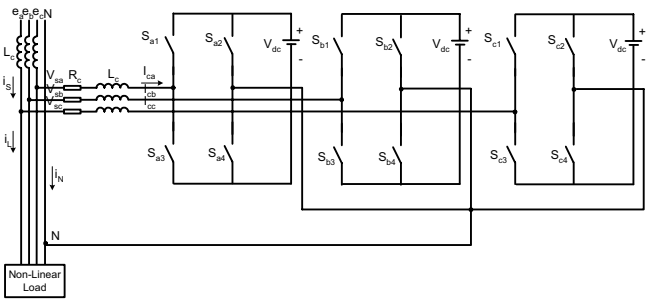


Fig. 2. Equivalent model of H-bridge tri-level inverter.

There are 3 cases in one arm of the tri-level converters such as positive, zero or negative switching function.

(i) if $S_a=1$, then $S_{a1}=0$, $S_{a2}=1$, $S_{a3}=1$, $S_{a4}=0$;
(ii) if $S_a=0$, then can be $S_{a1}=1$, $S_{a2}=1$, $S_{a3}=0$, $S_{a4}=0$ or $S_{a1}=0$, $S_{a2}=0$, $S_{a3}=1$, $Sa4=1$
(iii) if $S_a=-1$, then $S_{a1}=1$, $S_{a1}=0$, $S_{a1}=0$, $S_{a1}=1$;

Note that the possible values of S_a, S_b and S_c are *1*, *0* and *-1*. However, there are 2 possible situations when S_a changed from *1* to *0*. The possible results can be $S_{a1}=1$, $S_{a2}=1$, $S_{a3}=0$, $S_{a4}=0$ or $S_{a1}=0$, $S_{a2}=0$, $S_{a3}=1$, $S_{a4}=1$. In order to balance the switching activities in all the switches, a balanced switching table for phase **A** is obtained in Table 1, thus the average switching activities of the switches will be closer.

Table 1. Proposed switching table for phase **A**.

S_a	S_{a1}	S_{a2}	S_{a3}	S_{a4}	⇔	S_{a1}	S_{a2}	S_{a3}	S_{a4}
1⇔0	0	1	1	0	⇔	1	1	0	0
-1⇔0	1	0	0	1	⇔	0	0	1	1
1⇔-1	0	1	1	0	⇔	1	0	0	1

In Fig. 2, the boundary condition of S_{1a}, S_{2a} and S_{3a} is defined as:

$$\begin{cases} S_{a1}+S_{a2}+S_{a3}+S_{a4}=2 \\ S_{a1}=1 \ \ or \ \ 0, \ \ S_{a2}=1 \ \ or \ \ 0, \\ S_{a3}=1 \ \ or \ \ 0, \ \ S_{a4}=1 \ \ or \ \ 0. \end{cases} \tag{2}$$

It is worth to mention that when S_{a1} and S_{a2} are equal to 1, the values of S_{a3} and S_{a4} must be zero. The relationship among the ac-side compensating current and the terminal voltage of the inverter can be expressed in (3) according to Fig. 2.

$$\begin{cases} L_C \dfrac{di_{ca}}{dt} = -R_C \cdot i_{ca} - v_a + v_{sa} \\ L_C \dfrac{di_{cb}}{dt} = -R_C \cdot i_{cb} - v_b + v_{sb} \\ L_C \dfrac{di_{cc}}{dt} = -R_C \cdot i_{cc} - v_c + v_{sc} \end{cases} \tag{3}$$

By using the switching functions, the relation between the terminal voltage (V_a, V_b, V_c) and the dc-link voltage set $v_{dc1}= v_{dc2}= v_{dc}$ can be expressed in (4).

$$\begin{cases} V_a = S_{a2} \cdot S_{a3} \cdot v_{dc} - S_{a1} \cdot S_{a4} \cdot v_{dc} \\ V_b = S_{b2} \cdot S_{b3} \cdot v_{dc} - S_{b1} \cdot S_{b4} \cdot v_{dc} \\ V_c = S_{c2} \cdot S_{c3} \cdot v_{dc} - S_{c1} \cdot S_{c4} \cdot v_{dc} \end{cases} \tag{4}$$

A generalized mathematical model of the tri-level converter in three-phase four-wired systems can be established as follows:

$$Z\dot{X} = AX + BU \tag{5}$$

where

$$A = \begin{bmatrix} -R_C & 0 & 0 & -S_{a2} \cdot S_{a3} & S_{a1} \cdot S_{a4} \\ 0 & -R_C & 0 & -S_{b2} \cdot S_{b3} & S_{b1} \cdot S_{b4} \\ 0 & 0 & -R_C & -S_{c2} \cdot S_{c3} & S_{c1} \cdot S_{c4} \end{bmatrix}$$

$$X = [i_{ca} \ \ i_{cb} \ \ i_{cc} \ \ V_{dc1} \ \ V_{dc2}]^T \qquad B = diag[1 \ \ 1 \ \ 1]$$

$$U = [V_{sa} \ \ V_{sb} \ \ V_{sc}]^T \qquad Z = diag[L_C \ \ L_C \ \ L_C]$$

Due to three-phase symmetrical properties, the model equations are valid for both S_b and S_c in phase **B** and **C**, respectively.

3. 3-D PWM TECHNIQUE WITH SIGN CUBICAL HYSTERESIS CONTROL STRATEGY

In three-phase three-wired systems, there are many researches focusing on the PWM techniques such as the Sinusoidal PWM, Hysteresis Control PWM and Space Vector PWM etc. however, all of them are only investigated in 2-dimensional aspect. Only 2-D PWM cannot be utilized to solve the issues in three-Phase four-Wired Systems. The mathematical model of 3-D PWM is reviewed in this section.

The instantaneous voltage in *α-β-0* frame can be transferred from *a-b-c* frame, as expressed by

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{6}$$

The instantaneous voltage vector can be given by

$$V_s = \sqrt{\frac{2}{3}} (V_{SA} + \alpha \cdot V_{SA} + \alpha^2 \cdot V_{SC}) \tag{7}$$

where

$$\alpha = e^{j(2\pi/3)}, \qquad \alpha^2 = e^{-j(2\pi/3)}$$

According to the switching functions in (1), equation (7) can be expressed in *α-β-0* frame as given by:

$$V_s = V_{dc} \begin{bmatrix} i\sqrt{\frac{2}{3}} \left(S_\alpha - \frac{1}{2} \cdot S_b - \frac{1}{2} \cdot S_c \right) + \\ j \frac{1}{\sqrt{2}} (S_b - S_c) + k \left(\frac{1}{\sqrt{3}} (S_\alpha + S_b + S_c) \right) \end{bmatrix} \tag{8}$$

Equation (8) can be re-expressed as:

$$V_s = V_{dc} \left[i\sqrt{\frac{2}{3}} S_\alpha + j \frac{1}{\sqrt{2}} S_\beta + k \frac{1}{\sqrt{3}} S_0 \right] \tag{9}$$

where

$$S_a = S_a - \frac{1}{2} S_b - \frac{1}{2} S_c$$
$$S_\beta = S_b - S_c$$
$$S_0 = S_a + S_b + S_c$$

If the network has accessible neutral wire, a zero-sequence current component can exist. It is desired that the load current zero-sequence component can be compensated by the power quality compensator. For these cases, the zero-sequence converter current component, as well as the other components, must be controlled also. Fig. 3 shows the space vector allocation for tri-level inverter in *α-β-0* frame. According to (9), there are totally 27 possible vectors in tri-level inverter. They can be classified as four types: large-voltage, medium-voltage, small-voltage, and zero-voltage as listed in Table 2 [5]. Due to the special vectors problem [5], there are 6 operations that the compensation improves one direction will increase dedicated error in another direction since it is not a one-

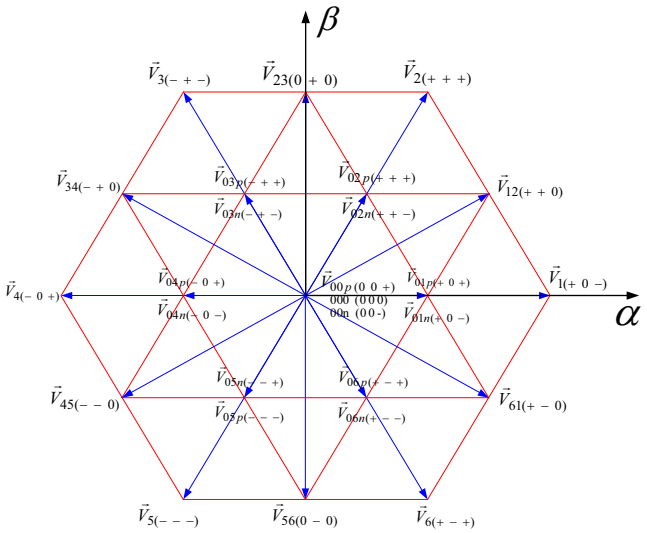


Fig. 3. Tri-level voltage vector allocation *α-β-0* frame.

to-one mapping relationship. This error can be solved by using cylindrical coordinate control strategy [9].

The sign cubical hysteresis current controller is studied in this section to control a tri-level 3-D voltage inverter for three-phase four-wired systems. The conception of sign cubical hysteresis control technique is shown in Fig. 4. The hysteresis limits of $\Delta\alpha$, $\Delta\beta$ and $\Delta 0$ can be equal to each other ($\Delta\alpha=\Delta\beta=\Delta 0$) so as to have a cubical controlling environment. There are 3 voltage levels {-1, 0, 1} in a tri-level voltage inverter. When the difference between the reference signal and actual input signal is larger than the hysteresis limited value, it will trigger to either positive or negative. However, when the difference is tolerable in the hysteresis limit, there will be the zero level. Fig. 5 shows the entire control strategy. The difference between the current reference and the actual load current would be the signal to compare with the injected current signal,

$$i^{*}_{\alpha\beta 0} = i^{reference}_{\alpha\beta 0} - i^{load}_{\alpha\beta 0} \tag{10}$$

$i^{reference}_{\alpha\beta 0}$ is the reference signal that can be obtained by instantaneous reactive power compensation technique, $i^{load}_{\alpha\beta 0}$ is the actual load current that may be distorted by non-linear or

Table 2. Space-vector control table.

	S_α	S_β	S_0	S_a	S_b	S_c		S_α	S_β	S_0	S_a	S_b	S_c	S_a	S_b	S_c
$\vec{V}_{02n}$	+	+	-	0	0	-1	$\vec{V}_{000}$	0	0	0	0	0	0			
$\vec{V}_{06n}$	+	-	-	0	-1	0	$\vec{V}_{1}$	+	0	0	1	-1	-1			
$\vec{V}_{03p}$	-	+	+	0	1	0	$\vec{V}_{4}$	-	0	0	-1	1	1			
$\vec{V}_{05p}$	-	-	+	0	0	1	$\vec{V}_{23}$	0	+	+	0	1	-1			
$\vec{V}_{12}$	+	+	0	1	0	-1	$\vec{V}_{23}$	0	+	-	0	1	-1			
$\vec{V}_{61}$	+	-	0	1	-1	0	$\vec{V}_{56}$	0	-	-	0	-1	1			
$\vec{V}_{34}$	-	+	0	-1	1	0	$\vec{V}_{56}$	0	-	+	0	-1	1			
$\vec{V}_{45}$	-	-	0	-1	0	1										
$\vec{V}_{23}$	0	+	0	0	1	-1	$\vec{V}_{2}/\vec{V}_{02p}$	+	+	+	1	1	-1	1	1	0
$\vec{V}_{56}$	0	-	0	0	-1	1	$\vec{V}_{6}/\vec{V}_{06p}$	+	-	+	1	-1	1	1	0	1
$\vec{V}_{01p}$	+	0	+	1	0	0	$\vec{V}_{3}/\vec{V}_{03n}$	-	+	-	-1	1	-1	-1	0	-1
$\vec{V}_{04n}$	-	0	-	-1	0	0	$\vec{V}_{5}/\vec{V}_{05n}$	-	-	-	-1	-1	1	-1	-1	0
$\vec{V}_{00p}$	0	0	+	1	1	1	$\vec{V}_{1}/\vec{V}_{01n}$	+	0	-	1	-1	-1	0	-1	-1
$\vec{V}_{00n}$	0	0	-	-1	-1	-1	$\vec{V}_{4}/\vec{V}_{04p}$	-	0	+	-1	1	1	0	1	1

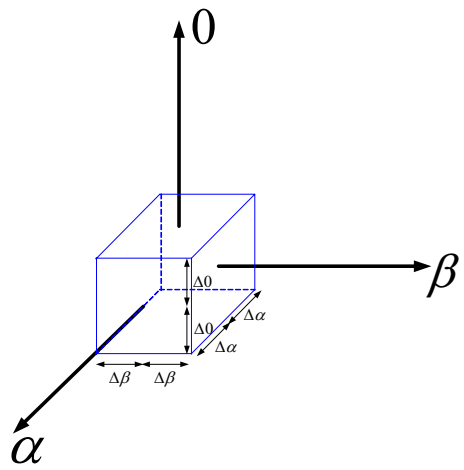


Fig. 4. Conception of sign cubical hysteresis control.

unsymmetrical load, and the difference between the reference signal and load current signal will be the tracking current ($i^{*}_{\alpha\beta 0}$) that should be injected by the inverter,

$$\Delta i_{\alpha\beta 0} = i^{*}_{\alpha\beta 0} - i_{c\alpha\beta 0} \tag{11}$$

The difference between the tracking current ($i^{*}_{\alpha\beta 0}$) and the coupling current $i_{c\alpha\beta 0}$ between the inverter and the load terminal will be the control signal ($\Delta i_{\alpha\beta 0}$) to the controller to control the action of inverter.

4. SIMULATION RESULTS

In Fig. 5, there is a switch in the signal-path that the injected current from the three-level inverter into the network can be detected. In this case, that switch could determine the switching frequency of the switching device, such as: IGBT. The switching functions of S_a, S_b and S_c can be adjusted from one state to another, and the speed of state change depends on the sampling rate of this switch. However, the systems performance will be affected by the sampling rate, the inductance and resistance values of the coupling transformer, voltage difference between the terminals of the inverter, the coupling point with the network, and also the values of the hysteresis limit. The simulation is conducted in MATLAB/SIMULINK to verify the functionality and

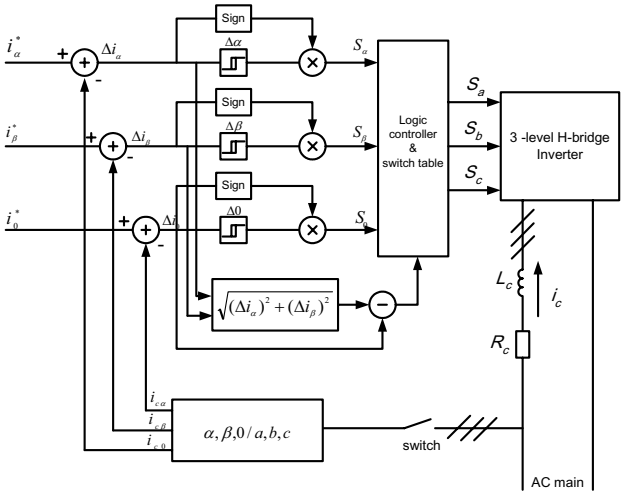
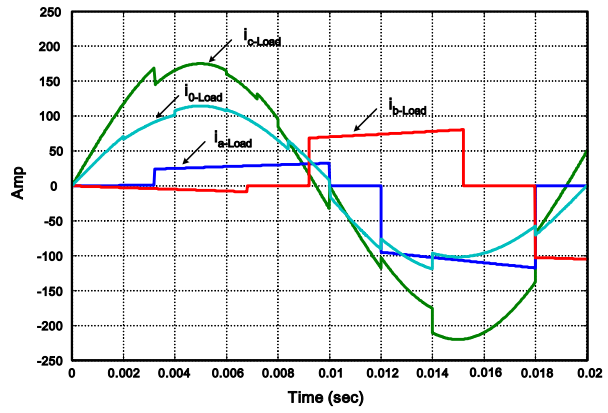
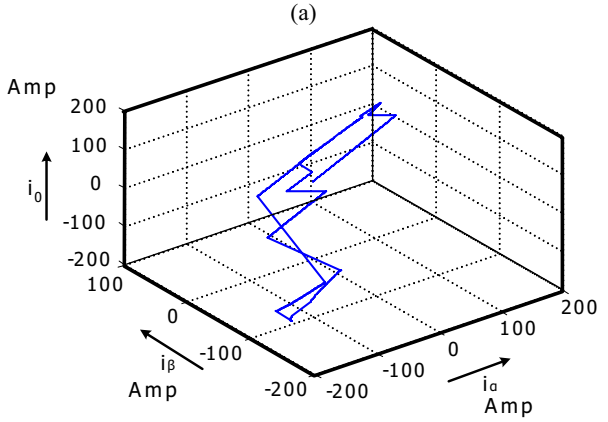


Fig. 5. Control strategy.

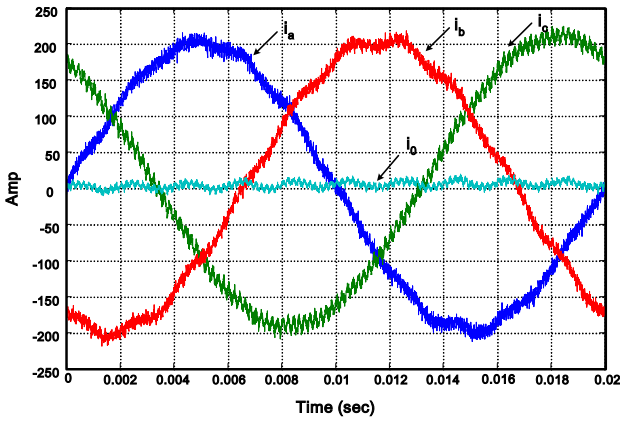


(a)

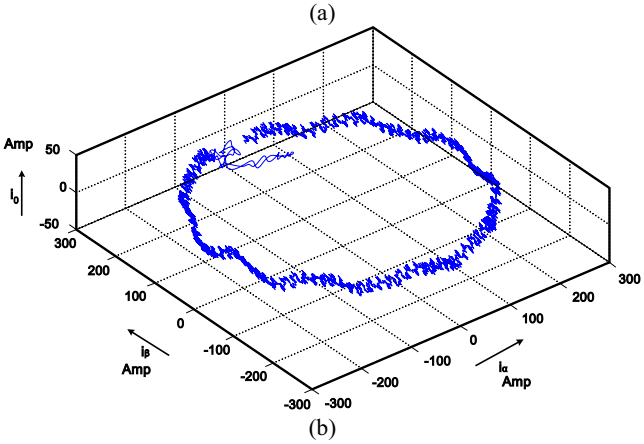


(b)

Fig. 6. Unbalance case of three-phase and neutral line load currents. (a) Time domain. (b) *α-β-0* domain.



(a)



(b)

Fig. 7. Compensated three-phase and neutral line source currents. (a) Time domain. (b) *α-β-0* domain.

performance of the tri-level H-bridge inverters, which acts as a power quality compensator for three-phase four-wired systems. Suppose there are three-phase unbalance load currents with 50 Hz as shown in Fig. 6(a), then the corresponding expression in *α-β-0* domain will be no longer a pure horizontal circle as shown in Fig. 6(b). However, when a tri-level H-bridge inverter is applied to compensate the source currents by using 3-D PWM with sign cubical hysteresis control operating in 20 kHz. Both the three-phase and neutral lines are highly improved in terms of total harmonic distortion (THD) and ripple, as shown in Fig. 7(a) and 7(b) in time and *α-β-0* domain respectively. Thus, the result verifies both the proposed model and the controlling technique are capable to compensate the heavy distorted three-phase and neutral line source currents simultaneously for three-phase four-wired systems.

5. CONCLUSIONS

A novel power quality compensator, constructed by H-bridge tri-level inverter with 3-D PWM control, has been proposed for three-phase four-wired systems. The mathematical model of such compensator and an enhanced switching table that balances the switching frequency of the switches were presented. With the sign cubical hysteresis control strategy, the simulation results verified that the current imbalance between the three-phase power lines as well as the neutral line due to non-linear loadings was effectively reduced. Thus, for three-phase four-wired systems, this highly expandable H-bridge tri-inverter with 3-D PWM control can be an attractive alternative of the widely utilized diode-clamped one, which suffers from the nature problem of DC-source unbalancing.

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