A 3-D Generalized Direct PWM Algorithm for Multilevel Converters

Ning-Yi Dai, *Student Member, IEEE*, Man-Chung Wong, *Member, IEEE*, Yuan-Hua Chen, and Ying-Duo Han, *Senior Member, IEEE*

***Abstract*—A three-dimensional (3-D) generalized direct pulse width modulation (PWM) algorithm is proposed for multilevel converters in a three-phase, four-wire system. It is proved to be equivalent to the newly proposed generalized 3-D space vector modulation (SVM). However, the direct PWM greatly simplifies the calculation process and is much easier to implement in digital controllers. The direct PWM can be used in all applications needing a 3-D control vector, such as active filters, uninterruptible power supplies, etc. Simulation and experimental results are given to show the validity of the proposed control strategy.**

***Index Terms*—3-D direct PWM, multilevel converters, three-phase four-wire system.**

I. Introduction

MULTILEVEL converters are becoming increasingly popular for medium- and large-capacity power quality compensators. They reduce voltage stress across the switches and improve harmonic contents of the voltage source inverter (VSI) by selecting appropriate switching vectors. The voltage stress decrease leads to a corresponding decrease of $\mathrm{dv/dt}$, which can reduce electromagnetic interference (EMI).

When compared with two-level, three-leg center-split inverters, the two-level, four-leg inverter is preferred by most of the researchers, as it only slightly increases the initial cost and avoids the troublesome issue of controlling the dc capacitor voltage unbalance. However, as the level of the inverter increases, the initial cost of adding an extra leg quickly increases. The number of available space vectors of an n-level, four-leg inverter is n times an n-level, three-leg inverter, which dramatically increases the complexity of the PWM control. In addition, both the three-leg and the four-leg, multilevel inverter need to implement the dc capacitor voltage variation control. Hence, the three-leg inverter has more advantages in multilevel systems. A dc voltage control strategy for a three-level, neutral point clamped (NPC) inverter has been discussed in [1].

Recently, several two-dimensional (2-D) space vector modulation (SVM) algorithms have been proposed for three-leg, multilevel converters [2]–[7]. In the 2-D SVM for three-phase, three-wire voltage source converters, the output phase-to-phase voltage can be controlled to be sinusoidal. Because the α-β transformation, which defines the 2-D space vectors, is not definitely reversible, one space vector in the α-β coordinates may correspond to a group of vectors in the a-b-c coordinates. If these vectors are decomposed to positive-, negative- and zero-sequence components, results indicate that their positive-sequence and negative-sequence components are the same. Only the amplitude of the zero-sequence component is different. Hence, the phase-to-neutral reference voltage is not necessarily sinusoidal in a 2-D SVM. Harmonics of triple orders can be added to the reference voltage vectors without affecting the α-β components [8]. As a result, the SVM can increase 15% of the dc voltage utilization compared with the sinusoidal PWM, which is implemented in per-phase mode.

It is natural to extend the 2-D space to the three-dimensional (3-D) space when the multilevel converter is connected to a three-phase, four-wire system. The reference vectors are not on a plane if the system is unbalanced or if there is a zero sequence or triple harmonics. The phase-to-neutral voltage of the converters must be sinusoidal in a three-phase, four-wire system. Hence, the dc voltage utilization cannot be increased by adding third harmonics to the phase-to-neutral reference voltage. Since the α-β-0 transformation is definitely reversible, both a-b-c coordinates and α-β-0 coordinates can be chosen to define the space vectors and to implement 3-D SVM control.

The 3-D SVM is first proposed in α-β-0 coordinates since it is straightforward to extend the α-β plane to the α-β-0 3-D coordinates for expressing 3-D vectors [9]–[11]. 3-D SVM in a-b-c coordinates has also been proposed [12]–[15], among which a generalized 3-D SVM for multilevel converters was proposed in 2003 [12]. The reference voltage vector is decomposed to an offset vector and a two-level vector in the generalized 3-D SVM. Important issues for the 3-D SVM, such as determination of switching sequence schemes and calculation of dwell time, are all done by a general two-level 3-D SVM. Although this PWM method is totally implemented in a-b-c coordinates, it still follows the conventional practice in SVM: the two-level space-vector cube is split into six tetrahedrons and subsequently the dwell time of each neighboring vector is calculated. The computational cost is high.

In this paper, a generalized direct PWM method is proposed, in which the switching state and the pulse width of each phase is directly determined in terms of the normalized reference voltage vector. It is proved that the modulation outputs of the direct PWM and the newly proposed 3-D SVM in the a-b-c coordinates [12] are the same when the reference voltage vector is the same. The computational cost of the direct PWM is much lower because the case determination chart and switching time table

Manuscript received February 3, 2005; revised April 25, 2005. This paper was recommended by Associate Editor L. M. Tolbert.

N.-Y. Dai and M.-C. Wong are with the Faculty of Science and Technology, University of Macau, Macau, China (e-mail: ya37404@umac.mo).

Y.-H. Chen is with the Department of Electrical Engineering, Tsinghua University, Beijing, China.

Y.-D. Han is with the Faculty of Science and Technology, University of Macau, Macau, China and also with the Department of Electrical Engineering, Tsinghua University, Beijing, China.

Digital Object Identifier 10.1109/LPEL.2005.855112

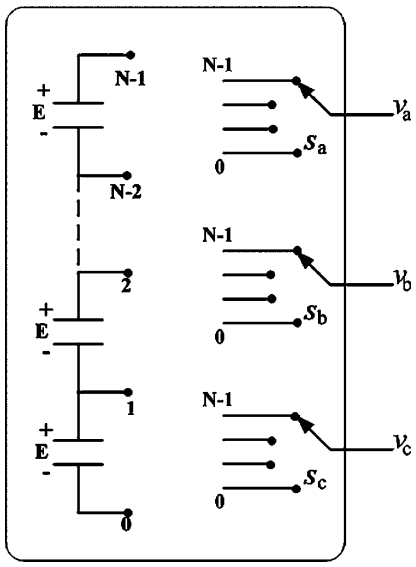

Fig. 1. Equivalent model of N-level VSI.

in [12] are not needed. The low computational cost is always the same and is independent of the number of converter levels. So, it can be used as a generalized PWM method for generating 3-D control vectors. Simulation and experimental results are given to show the validity of the proposed control strategy.

II. Generalized Direct PWM Method

An equivalent model for an N-level voltage source inverter is shown in Fig. 1 [5]. The phase output voltage can be expressed as

$$V_j = S_j \cdot E \qquad j = a,b,c \text{ and } 0 \le S_j \le N-1 \tag{1}$$

where $\boldsymbol{S}_j$ denotes the switching state of the corresponding phase and E denotes the dc voltage of one level. In this letter, all the voltage vectors are represented per unit, i.e., normalized by E, so that the output voltage of each phase can be expressed as

$$v_j = S_j \qquad j = a,b,c \text{ and } 0 \le S_j \le N-1. \tag{2}$$

The reference voltage vector is also normalized by E, as expressed in (3):

$$\vec{v}_{ref} = \frac{\vec{V}_{ref}}{E}. \tag{3}$$

In the generalized direct PWM, the desired output voltage vector is decomposed into two components: the offset voltage vector and the two-level voltage vector. The two-level voltage vector will be used to directly determine the final pulse width, which is totally different from the method in [12].

$$\vec{v}_{ref} = \vec{v}_{offset} + \vec{v}_{twol}. \tag{4}$$

It can also be expressed in a-b-c coordinates as

$$\begin{bmatrix} v_{refa} \\ v_{refb} \\ v_{refc} \end{bmatrix} = \begin{bmatrix} v_{offseta} \\ v_{offsetb} \\ v_{offsetc} \end{bmatrix} + \begin{bmatrix} v_{twola} \\ v_{twolb} \\ v_{twolc} \end{bmatrix}$$

$$\text{where} \begin{bmatrix} v_{offseta} \\ v_{offsetb} \\ v_{offsetc} \end{bmatrix} = \begin{bmatrix} INT(v_{refa}) \\ INT(v_{refb}) \\ INT(v_{refc}) \end{bmatrix}.$$

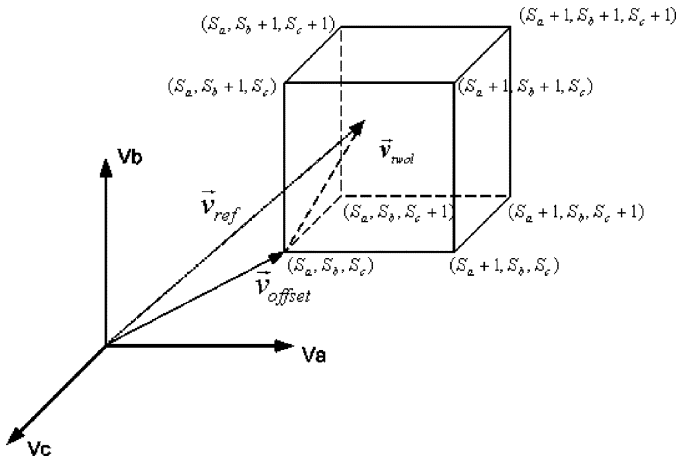

Fig. 2. Decomposition of reference voltage vector.

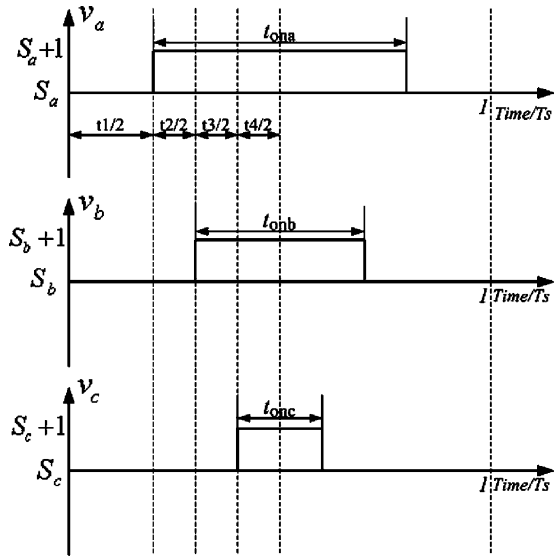

Fig. 3. PWM output of one sampling period.

$INT()$ removes the fractional part of the real input data. If $(v_{offseta}, v_{offsetb}, v_{offsetc})$ equals (S_a, S_b, S_c), the reference voltage vector locates inside the two-level space vector allocation formed by $(S_a, S_b, S_c)(S_a+1, S_b, S_c)$, (S_a, S_b+1, S_c), (S_a, S_b, S_c+1), (S_a+1, S_b+1, S_c), (S_a+1, S_b, S_c+1), (S_a, S_b+1, S_c+1) and (S_a+1, S_b+1, S_c+1), as illustrated in Fig. 2. In order to reduce the dv/dt of the output voltage in multilevel PWM control, the output voltage changes only one level in one switching period. So the two switching states of one phase are $\boldsymbol{S}_j$ and $\boldsymbol{S}_j+1$ $(j=a,b,c)$ in a switching period.

The direct PWM is based on the volt-second approximation just as in conventional SVM. The voltage is approximated in per-phase mode in a-b-c coordinates, i.e., the reference voltage vector is synthesized in phases A, B and C independently, as illustrated in (5):

$$v_{refj} \cdot T_S = v_{offsetj} \cdot t_{offj} + (v_{offsetj}+1) \cdot t_{onj} \qquad j=a,b,c \tag{5}$$

where T_S is the sampling period, t_{offj} is the dwell time of the output state $\boldsymbol{S}_j$, t_{onj} is the dwell time of the output state $\boldsymbol{S}_j+1$,

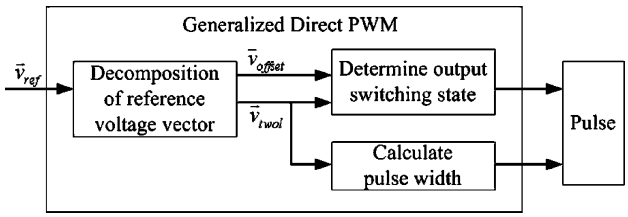

Fig. 4. Flow chart of the direct PWM method.

and $t_{offj}+t_{onj}=T_S\,(j=a,b,c\,)$. If $\vec{v}_{offsetj}\cdot T_S$ is subtracted from both sides of (5), (6) can be obtained:

$$(v_{refj}-v_{offsetj})\cdot T_S = v_{offsetj}\cdot t_{offj} + (v_{offsetj}+1)\cdot t_{onj} - v_{offsetj}\cdot(t_{offj}+t_{onj}) = t_{onj} \quad (6)$$

$$\text{Since } v_{refj}-v_{offsetj}=v_{twolj} \qquad j=a,b,c$$

$$v_{twolj}=\frac{t_{onj}}{T_S} \qquad j=a,b,c \quad (7)$$

$$\text{and} \quad 1-v_{twolj}=\frac{t_{offj}}{T_S}. \quad (8)$$

The t_{onj} is the pulse width of the corresponding phase j($j=a,b,c\,$), as shown in Fig. 3. The normalized two-level reference voltage vector v_{twolj} in (7) equals the normalized pulse width of the respective phase.

No matter what PWM control strategies are used, the final trigger signals are sending to the switches of the respective phase independently. After the t_{onj} of each phase is determined, the modulation output of the inverter can be generated. The proposed PWM control method is called "direct PWM" because it is implemented by directly calculating the pulse width of each phase. It is mentioned in [12] that 69 instructions and a maximum of three comparisons are needed for calculating the 3-D state vectors and duty-cycles. However, only nine instructions are needed to calculate the pulse widths of three-phases and no comparisons are needed in the proposed direct PWM.

III. Equivalence to the 3-D SVM in a-b-c Coordinates

The flow chart of the direct PWM is shown in Fig. 4, which is the same as that of the generalized 3-D SVM in a-b-c coordinates [12]. A general two-level 3-D SVM is employed to calculate the dwell time of each switching state in [12], in which the two-level space vector allocation is divided to six tetrahedrons and the two-level reference voltage vector is synthesized by four neighboring vectors.

$$\vec{v}_{twol}\cdot T_S = \vec{v}_1 t_1 + \vec{v}_2 t_2 + \vec{v}_3 t_3 + \vec{v}_4 t_4 \quad (9)$$

$$\text{and} \;\; t_1+t_2+t_3+t_4 = T_S. \quad (10)$$

Equation (9) can also be expressed as

$$\begin{bmatrix} v_{twola} \\ v_{twolb} \\ v_{twolc} \end{bmatrix} \cdot T_S = \begin{bmatrix} S_a^1 & S_a^2 & S_a^3 & S_a^4 \\ S_b^1 & S_b^2 & S_b^3 & S_b^4 \\ S_c^1 & S_c^2 & S_c^3 & S_c^4 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix}. \quad (11)$$

After the dwell time of each neighboring vector is obtained, the final output of the inverter can be generated. This is also illustrated in Fig. 3. Since $\vec{v}_1$, $\vec{v}_2$, $\vec{v}_3$ and $\vec{v}_4$ are space vectors of a two-level space vector allocation, its normalized output S_j^m ($j=a,b,c$; $m=1,2,3,4$) can be only "0" or "1". The pulse width of each phase is the summation of the dwell time of the vectors, whose output in that phase equals 1. That is to say, if S_x^m equals 1, the dwell time t_m of this vector $\vec{v}_m$ is added to the pulse width. If $S_x^m=0$, t_m is not added to pulse width t_{onj}. So S_x^m can also be used as the coefficient for calculating the pulse width. If phase A is considered as an example, $t_{ona}=S_a^1t_1+S_a^2t_2+S_a^3t_3+S_a^4t_4$. The following equation can be obtained:

$$\begin{bmatrix} t_{ona} \\ t_{onb} \\ t_{onc} \end{bmatrix} = \begin{bmatrix} S_a^1 & S_a^2 & S_a^3 & S_a^4 \\ S_b^1 & S_b^2 & S_b^3 & S_b^4 \\ S_c^1 & S_c^2 & S_c^3 & S_c^4 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix}. \quad (12)$$

Equation (7) can be deduced again if (11) is compared with (12), which indicates that the normalized two-level reference voltage vector equals the normalized pulse width of the respective phase. Therefore, the time-consuming mid-steps, such as neighboring vectors' determination and dwell time calculations, can all be eliminated. Direct PWM can replace 3-D SVM because the two PWM methods generate the same output waveform when the same reference voltage vector is applied.

IV. Simulation and Experimental Results

A prototype of the three-level neutral point clamped (NPC) inverter has been developed. It is controlled by a fixed point DSP (TMS320F2407, @30 MHz). Simulation results and experimental results are given to show the validity of the proposed direct PWM. The system configuration is shown in Fig. 5. The sampling frequency is 5 kHz.

Simulation and experimental results are shown in Figs. 6 and 7, respectively. The three-phase unbalanced voltage is generated. The third harmonic is added to the reference voltage of phase A. The inverter output voltage of phase A, which is denoted as Ea in Fig. 5, and the three-phase voltages across the loads are shown in Fig. 6. The three-phase voltages and neutral current are shown in Fig. 7. The recorded voltage total harmonic distortin (THD) values in the simulation and experiment are listed in Table I. Since the voltage is measured by using a Hall-effect voltage transducer, its amplitude is greatly reduced when it is recorded in the oscilloscope.

When Fig. 6 is compared with Fig. 7, results indicate that the simulation and experimental results are matched. Furthermore, it is proved that direct PWM can trace arbitrary reference voltages and can be used in a three-phase, four-wire system with a nonzero neutral current. Hence, it can be applied to applications where either pure sinusoidal or nonsinusoidal output needs to be generated.

V. Conclusion

Generalized direct PWM omits the troublesome determination of sextant and switching time calculations in the 3-D SVM [12], thus providing a simpler way to implement 3-D control for multilevel converters. The computational cost is always the same for inverters of different levels. This technique can be used as a modulation method in all applications needing to generate

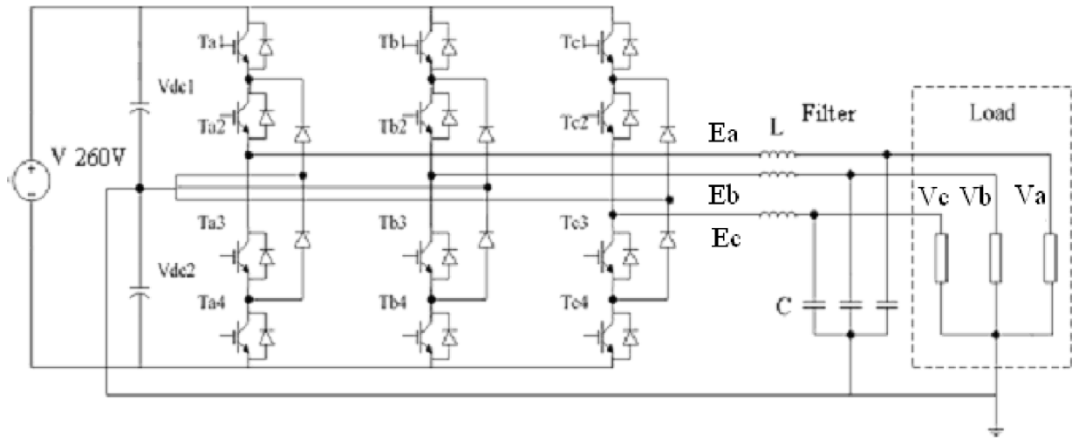

Fig. 5. System configuration of a three-phase, four-wire active power filter.

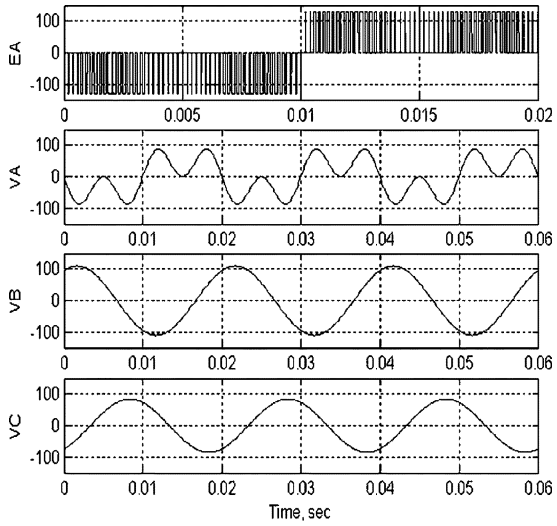

Fig. 6. Simulation results.

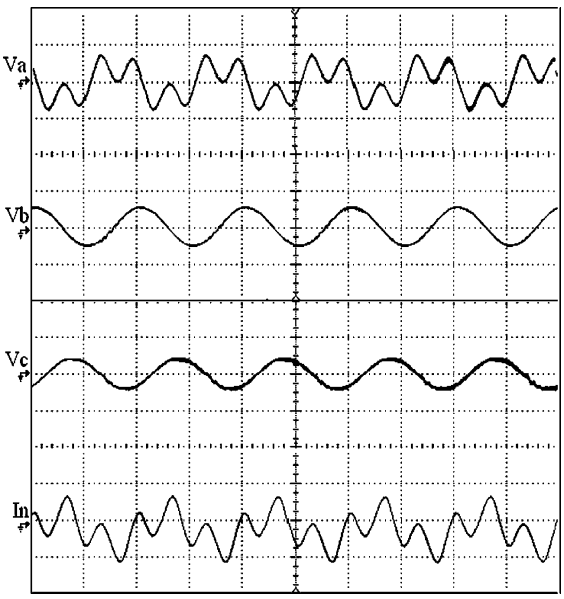

Fig. 7. Experimental results.

a 3-D space vector, such as UPS, APF, etc. Furthermore, it is very useful for controlling inverter outputs online.

TABLE I
THD OF THREE-PHASE VOLTAGE

	A	B	C
Voltage THD in simulation	100%	1.166%	1.178%
Voltage THD in experiment	99.40%	2.706%	3.599%

REFERENCES

[1] M.-C. Wong, N.-Y. Dai, and Y.-D. Han, "Study of tri-level neutral point clamped inverter for 3-phase 3-wire and 3-phase 4-wire applications," in *Proc. IEEE PEDS 2003*, vol. 1, 2003, pp. 380–385.

[2] J. H. Seo, C. H. Choi, and D. S. Hyun, "A new simplified space-vector PWM method for three-level inverter," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 545–550, Jul. 2001.

[3] Y. Liu, X. Wu, and L. Huang, "Implementation of three-level inverter using a novel space vector modulation algorithm," in *IEEE PowerCon2002*, vol. 1, 2002, pp. 606–610.

[4] A. R. Bakhshai, H. R. S. Rad, and G. joos, "Space vector modulation based on classification method in three-phase multi-level voltage source inverters," in *IEEE IAS Annu. Meeting*, vol. 1, 2001, pp. 597–602.

[5] Q. Song, W. Liu, G. Yan, and Y. Chen, "DSP-based universal space vector modulator for multi-level voltage-source inverters," in *Proc. IEEE IECON 2003*, vol. 2, 2003, pp. 1727–1732.

[6] Y.-H. Chen, "Investigation of Control Strategies for Hybrid Multilevel Inverter," Doctor Degree, Tsinghua Univ., Beijing, China, 2003.

[7] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Applicat.*, vol. 37, no. 2, pp. 637–641, Mar.-Apr. 2001.

[8] H. W. Van der Broeck, H.-C. Skudelny, and G. V. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Trans. Ind. Applicat.*, vol. 24, no. 1, pp. 142–150, Jan.-Feb. 1988.

[9] C. Liu, D. Peng, and R. Zhang, "Four-legged converter 3-D SVM scheme over-modulation study," in *Proc. IEEE APEC 2000*, vol. 1, 2000, pp. 562–568.

[10] R. Zhang, V. H. Prasad, D. Boroyevich, and F. C. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," *IEEE Trans. Power Electron.*, vol. 17, no. 3, pp. 314–326, May 2002.

[11] N. Y. Dai, M. C. Wong, and Y. D. Han, "Three-dimensional space vector modulation with DC voltage variation control in a three-leg center-split power quality compensator," *Proc. Inst. Elect. Eng., Electr. Power Appl.*, vol. 151, no. 2, pp. 198–204, Mar. 2004.

[12] M. M. Prats, L. G. Franquelo, R. Portillo, J. I. Leon, E. Galvan, and J. M. Carrasco, "A 3-D space vector modulation generalized algorithm for multi-level converters," *IEEE Power Electron. Lett.*, vol. 1, no. 4, pp. 110–114, Dec. 2003.

[13] M. M. Prats, L. G. Franquelo, J. I. Leon, R. Portillo, E. Galvan, and J. M. Carrasco, "A SVM-3D generalized algorithm for multilevel converters," in *Industrial Electronics Soc., 2003. IECON '03. The 29th Annu. Conf. IEEE*, vol. 1, 2003, pp. 24–29.

[14] M. M. Prats, J. M. Carrasco, and L. G. Franquelo, "Effective algorithm for multilevel converter with very low computational cost," *Electron. Lett.*, vol. 38, pp. 1398–1400, 2002.

[15] M. A. Perales, M. M. Prats, R. Portillo, J. L. Mora, J. I. Leon, and L. G. Franquelo, "Three dimensional space vector modulation in abc coordinates for four-leg voltage source converters," *IEEE Power Electron. Lett.*, vol. 1, no. 4, pp. 104–109, Dec. 2003.