DCM operation analysis of KY converter

Wen-Liang Zeng, Chi-Seng Lam✉, Wen-Ming Zheng, Sai-Weng Sin, Ning-Yi Dai, Man-Chung Wong, Seng-Pan U and Rui Paulo Martins

A KY converter has the characteristics of non-pulsating output current, low-output voltage ripple and no right-half plane zero in continuous conduction mode which can overcome the drawbacks of the conventional boost and buck–boost converters. However, when the KY converter is implemented into an integrated circuit, its discontinuous conduction mode (DCM) operation cannot be avoided due to a small-inductor value. The boundary for the DCM operation region, DCM dc voltage and small-signal transfer functions are proposed, which fill the gap of the DCM operation theory for the KY converter. Simulation results, using MATLAB and Cadence, are provided to verify the deduced DCM operation theory of the KY converter. The DCM closed-loop controller design can be achievable in future.

Introduction: Voltage boosting dc–dc converters are required in many computer, communication and consumer electronics products, such as MPEG-3 (MP3) players, personal digital assistants etc. For such applications, output voltage ripple and noise should be taken into consideration. As for conventional voltage-boosting converters, such as boost, buck–boost converters, their output currents are pulsating, thereby causing the output voltage ripple to be large [1]. Moreover, they have a right-half plane zero (RHPZ) in the continuous conduction mode (CCM), thereby lowering system stability and degrading the load transient response [2]. To overcome such drawbacks, a boost converter called a KY converter was proposed by Hwu and Yau [1] for power electronics applications. This converter comprises a switched-capacitor charge pump converter and a buck converter, and combines the advantages of both converters and exhibits the characteristics of non-pulsating output current, low-output voltage ripple and no RHPZ in CCM [1, 3]. Moreover, it always operates in CCM as claimed in [1, 3]. However, when the KY converter is implemented into a power management integrated circuit (IC), due to a small inductance, its discontinuous-conduction mode (DCM) operation cannot be avoided for longer battery life. This Letter presents a DCM operation analysis of the KY converter.

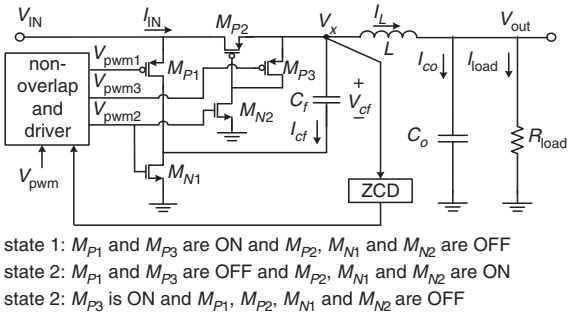

Fig. 1 *Proposed KY converter IC topology for DCM*

KY converter and its ideal equivalent circuits for DCM: Fig. 1 shows the proposed KY converter IC topology for DCM, where V_{IN} and V_{OUT} are the dc input and output voltages; C_f and V_{Cf} are the flying capacitor and its voltage ($V_{Cf} = V_{IN}$ in the ideal case [1]); L and C_O are the inductor and capacitor of the LC filter; R_{Load} is the load resistor; I_{IN}, I_{Load}, I_{cf}, I_L and I_{Co} are the input, load, flying capacitor, inductor and capacitor currents, respectively. The KY converter contains three power transistor switches (M_{P1}, M_{P2} and M_{N1}) and two control transistor switches (M_{P3} and M_{N2}). The V_{pwm1-3} signals via the non-overlapping and driver circuit are used to control these transistor switches, ZCD represents the zero current detector to trigger state 3 in Fig. 1. Fig. 2 shows the KY converter's idealised V_L and I_L waveforms for DCM.

Boundary between CCM and DCM of KY converter: The boundary between CCM and DCM can be defined when $D_2 = 0$ in Fig. 2. From Fig. 2, the peak inductor current ΔI_L can be deduced, then the average dc output load current I_{LoadB} at the boundary can be expressed as

$$I_{LoadB} = \frac{\Delta I_L}{2} = \frac{(2V_{IN} - V_{OUT})D}{2f_sL} \quad (1)$$

where f_s is the switching frequency and D is the duty cycle for state 1. At the boundary, the CCM dc voltage transfer function is $M_{VDC} = M_{VDC\_CCM} = V_{OUT}/V_{IN} = 1 + D$ [1]. By substituting M_{VDC_CCM} into (1), I_{LoadB} and the load resistance R_{LoadB} at the boundary are given by

$$I_{LoadB} = \frac{(1-D)D}{2f_sL} \quad (2)$$

$$R_{LoadB} = \frac{V_{OUT}}{I_{LoadB}} = \frac{2Lf_s(1+D)}{(1-D)D} \quad (3)$$

Fig. 3 shows the normalised load current $I_{LoadB}/(V_{out}/2f_sL)$ and load resistance $R_{LoadB}/2f_sL$ at the CCM/DCM boundary against D.

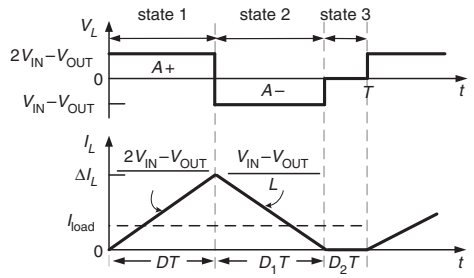

Fig. 2 *KY converter's idealised V_L and I_L waveforms for DCM*

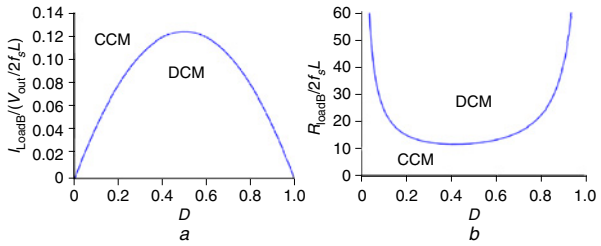

Fig. 3 *Normalised load current and load resistance at CCM/DCM boundary against D for KY converter. Fig. 3a: $I_{LoadB}/(V_{out}/2f_sL)$ against D; Fig. 3b: $R_{LoadB}/2f_sL$ against D*

DC voltage transfer function of KY converter for DCM: Its open-loop voltage gain under DCM can be deduced from Fig. 2, during the time interval $0 < t \le DT$ and $DT < t \le (DT + D_1T)$, states 1 and 2 of the KY converter are triggered. Applying the volt–second balance principle, $A^+ = A^-[(2V_{IN} - V_{OUT})DT = (V_{OUT} - V_{IN})D_1T]$ as shown in Fig. 2 can be obtained. This leads to the DCM dc voltage transfer function

$$M_{VDC} = M_{VDC\_DCM} = \frac{V_{OUT}}{V_{IN}} = \frac{2D + D_1}{D + D_1} \quad (4)$$

From Fig. 2 and with ΔI_L, the dc output load current I_{Load} is equal to the average value of the inductor current I_L, that is

$$I_{Load} = \frac{1}{T}\int_0^T I_L T\mathrm{d}t = \frac{(D+D_1)\Delta I_L}{2} = \frac{(2V_{IN} - V_{OUT})D(D+D_1)}{2f_sL} \quad (5)$$

Finding D_1 from (4) and substituting it into (5), then solving

$$M_{VDC}^2 + \left(\frac{D^2}{k} - 1\right)M_{VDC} - \frac{2D^2}{k} = 0 \quad (6)$$

where $k = (2Lf_s/R_{Load})$. The DCM dc voltage transfer function M_{VDC} is

$$M_{VDC} = M_{VDC\_DCM} = \frac{V_{OUT}}{V_{IN}} = \frac{(1 - (D^2/k)) + \sqrt{(D^4/k^2) + (6D^2/k) + 1}}{2} \quad (7)$$

Fig. 4 shows the plots of M_{VDC} against normalised load current $I_{Load}/(V_{out}/2f_sL)$ and load resistance $R_{Load}/2f_sL$ at different D for the lossless KY converter. The cross points 'X' in Fig. 4 are the simulation results using Cadence, which confirm the CCM and DCM boundary study (1)–(3) and the DCM M_{VDC} of the KY converter (7).

Small-signal transfer function of KY converter for DCM: To design a closed-loop controller under DCM, its DCM small-signal transfer

function is necessary. Following the same deduction method of the buck converter [4] and considering that the flying capacitor voltage V_{Cf} slightly deviates from the input voltage V_{IN} ($V_{Cf} \neq V_{IN}$) as in Fig. 5*a*, this voltage drop ΔV_{Cf} in one period T can be modelled as a voltage drop $\overline{\Delta V}_{Cf}$ on an equivalent resistor R_{eq}. Then, the small-signal model of the KY converter for DCM is shown in Fig. 5*b*.

The R_{eq} in one period can be calculated by the principle of charge conservation. The total charge ΔQ that flows away from C_f is equal to the total charge flowing into L, from Fig. 2, $\Delta Q = (DT \times \Delta I_L)/2$. With help of the average inductor current $\bar{I}_L$ in one period T (5), the flying capacitor voltage deviation ΔV_{Cf} shown in Fig. 5*a* is

$$\Delta V_{Cf} = \frac{\Delta Q}{C_f} = \frac{D\bar{I}_L}{f_s C_f (D + D_1)} \tag{8}$$

Considering an average ΔV_{Cf} value in one period, $\overline{\Delta V}_{Cf}$ can also be expressed as: $\overline{\Delta V}_{Cf} = R_{eq}\bar{I}_L$. From (8), R_{eq} can be obtained as

$$R_{eq} = \frac{\overline{\Delta V}_{Cf}}{\bar{I}_L} = \frac{D^2}{2 f_s C_f (D + D_1)} \tag{9}$$

Then, the modified DCM M_{VDC} for the KY converter becomes

$$M_{VDC} = M_{VDC\text{-}DCM} = \frac{-(kD^2b - k^2b - 4D^5) + \sqrt{(kD^2b - k^2b - 4D^5)^2 - 4(k^2b + D^5)(4D^5 - 2kD^2b)}}{2} \tag{10}$$

where $b = 2f_s C_f R_{Load}$. With the help of [4], replacing k_d and r in Fig. 5*b*, with the dc analysis values k and M_{VDC} (10), will lead, respectively, to

$$k_d = \frac{2V_{OUT}}{R_{Load}} \sqrt{\frac{2 - M_{VDC}}{kM_{VDC}(M_{VDC} - 1)}}, r = \frac{R_{Load}(2 - M_{VDC})(1 - M_{VDC})}{M_{VDC}} \tag{11}$$

Finally, the KY converter small-signal transfer function in DCM can be expressed as

$$G_{vd} = \frac{\hat{V}_{OUT}}{\hat{d}} = H_d \frac{1 + (s/s_{z1})}{1 + a_1 s + a_2 s^2} \tag{12}$$

where

$$H_d = k_d \frac{rR_{Load}}{r + R_{Load} + R_{eq} + r_L}, a_2 = LC_f \frac{r_c + R_{Load}}{r + R_{Load} + R_{eq} + r_L}$$

$$s_{z1} = \frac{1}{r_c C_f},$$

$$a_1 = \frac{L + C_f\left[(R_{Load} + r_c)(r + r_L + R_{eq}) + R_{Load} r_c\right]}{r + R_{Load} + R_{eq} + r_L},$$

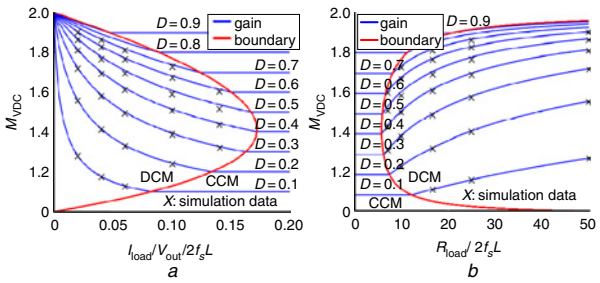

Fig. 4 *DC voltage transfer function M_{VDC} against normalised load current and load resistance at different D for lossless KY converter. Fig. 4a: M_{VDC} against $I_{Load}/(V_{out}/2f_sL)$; Fig. 4b: M_{VDC} against $R_{Load}/2f_sL$*

Simulation verification of small-signal transfer function of KY converter for DCM: The KY converter was built with the transistor level in 65 nm CMOS process; its bode plot data are obtained using the periodic AC analysis with the Cadence Spectre simulator. With a set of designed parameters ($V_{IN} = 1$ V, $f_s = 200$ MHz, $C_f = 5$ nF, $C_o = 15$ nF, $L = 5$ nH, $r_L = r_C = 20$ mΩ, $R_{Load} = 50$ Ω), Fig. 6 compares the simulated bode plots between the transfer function (12) and power stage (Fig. 1) when $D = 0.3$ and $D = 0.5$, respectively. The plots are consistent for frequencies smaller than one third of f_s, which is acceptable for the closed-loop controller design and also verified (12). The difference between them is due to the switch on resistance and the rise and fall times of the transistor switches, which are not considered in (12).

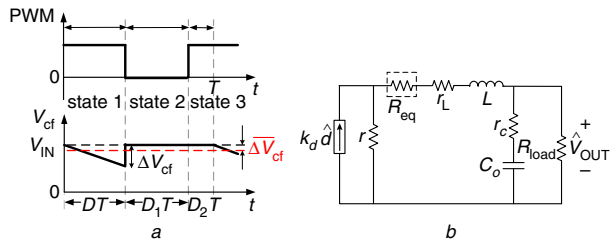

Fig. 5 *Small-signal model of KY converter for DCM. Fig. 5a: flying capacitor voltage V_{Cf} deviation phenomenon; Fig. 5b: small-signal model with V_{Cf} deviation consideration*

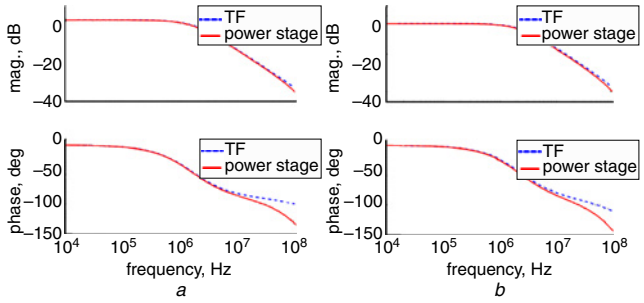

Fig. 6 *KY converter open-loop bode plot for DCM when D = 0.3 (Fig. 6a) and D = 0.5 (Fig. 6b)*

Conclusion: This Letter presents the DCM operation analysis of the KY converter. The theoretical equations deducted are important for the design of the DCM closed-loop controller of the KY converter IC. Simulation results using MATLAB and 65 nm CMOS technology in Cadence confirm the DCM theory.

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One or more of the Figures in this Letter are available in colour online.

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References

1 Hwu, K.I., and Yau, Y.T.: 'KY converter and its derivatives', *IEEE Trans. Power Electron.*, 2009, **24**, (1), pp. 128–137, doi: 10.1109/TPEL.2008.2009178
2 Kondrath, N., and Kazimierczuk, M.K.: 'Control-to-output transfer function of peak current-mode controlled PWM DC–DC boost converter in CCM', *Electron. Lett.*, 2011, **47**, (17), pp. 991–993, doi: 10.1049/el.2011.1011
3 Wang, F., Zhang, Y., and Ma, X.: 'Small signal transfer functions modelling and analysis for open loop KY converter'. Proc. IEEE Int. Symp. on Industrial Electronics (ISIE) 2013, Taipei, Taiwan, May 2013, pp. 1–4, doi: 10.1109/ISIE.2013.6563713
4 Vorperian, V.: 'Simplified analysis of PWM converters using model of PWM switch. II. Discontinuous conduction mode', *IEEE Trans. Aerosp. Electron. Syst.*, 1990, **26**, (3), pp. 497–505, doi: 10.1109/7.106127