Hybrid Cascaded Multilevel Converter for Medium-voltage Large-capacity Applications

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Abstract—**Multilevel converters are particularly suitable to be used in medium to high voltage applications, such as in a Railway Power Compensator (RPC), since they can give better quality outputs and reach higher voltage rates compared with two-level converters. In this paper, a novel 6-stage hybrid cascaded multilevel converter for medium-voltage large-capacity applications is proposed. It can reach the voltage rate of 30 kV with minimum step of 2 kV so that the RPCs using it can be connected directly to the traction system without coupling transformers. It is a 31-level converter, which could reduce the harmonic contents in the output waveforms. However, the number of cascaded stages of it is much less compared with the ones using traditional cascading methods. The corresponding control method for the proposed converter is also designed. Simulation and hardware testing results are also provided to show the validity of the proposed hybrid multilevel converter and its control strategy.**

Keywords—**hybrid cascaded multilevel converter; railway power compensator (RPC); direct-PWM; hybrid PWM**

I. INTRODUCTION

Multilevel converters can give output with more than two voltage levels, which enables the converter to give good quality outputs with lower switching frequencies. Moreover, it is easy for multilevel converters to realize high voltage and high power applications since they can be built in cascaded forms using several independent DC sources, and the voltage applied on each individual switching component need not be very high [1].

Trying to design multilevel converter with higher voltage and reduce the complexity of the structure is a main research direction for designing new multilevel converters. Recently, power converters that can work at voltage levels of several tens of kilovolts are needed in many new industrial fields. In order to achieve this goal, cascaded converter with more than ten or even twenty stages are needed. A large number of switching devices, drivers, and controllers are needed. The size, initial cost and complexity of the control circuits are increased as too many power switches are involved.

For example, cascaded multilevel converters were proposed to be used as the main circuit of railway power compensator (RPC) [2]. RPCs are connected to the traction power system, aiming at reducing the power quality problems such as harmonics, negative sequence current, large portion of reactive power caused by the traction loads [3, 4]. RPCs use power converters (rectifier + DC links + inverter) as the main circuit [5]. For normal trunk railway lines, the supply voltage of the railway's contact lines is usually 25 kV_{rms} ($\approx 35.355\ \text{kV}_{\text{peak}}$) [6]. So the required voltage rating of the power converters in the RPC may vary from 20kV to 40kV, according to different compensator configurations.Since the power converters used for RPC system need to reach such a high voltage level, RPCs using traditional multilevel converters cannot be connected to the traction system directly. They are connected by a linking transformer between them.

The use of traditional power converters and linking transformers causes several problems, which become more and more significant as the fast development and wide use of high speed trains and large load cargo trains. For example, the linking transformer can cause distortion to the compensation waveforms. The distortion caused by the transformer can change the waveform of the compensation voltage/current severely.So the use of traditional power converters and the existing of linking transformer can reduce the compensation effect and sometimes even cause the compensation to fail [1]. In order to improve the current design, a new multilevel converter that can reach the same voltage as the traction power system needs to be designed. As discussed before, cascaded multilevel converter is easy to realize high voltage and high power output since several independent converter stages can be cascaded to become a cascaded multilevel converter, and the total voltage is the sum of the DC voltage of all the stages [7, 8].

In this paper, a novel multilevel converter using IGCT and IGBT hybrid cascaded structure is proposed. The output voltage can reach 30 kV so that it can be directly connected to the traction power system without any linking transformer [9]. The design target of this multilevel converter is to make the structure as simple as possible and apply proper control algorithm so that the converter can give artificial output with good quality.

II. TOPOLOGY AND FEATURES

The structure of the proposed hybrid cascaded multilevel converter is shown in Fig. 1 (inverter parts). The converter is cascaded by 6 stages of 2H Bridges and the voltage of each stage is labeled in the circuit diagram.

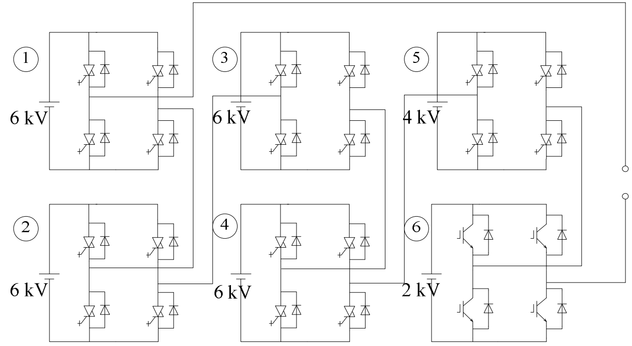

Figure 1: The structure of the proposed hybrid cascaded multilevel converter

In this design, stages 1~5 use IGCT bridges in order to increase the DC voltage level. But IGCT cannot operate in such high frequencies as IGBT (the maximum operation frequency of IGCT at such high power applications is usually 500 Hz and IGBT is 5 kHz [10]); this requirement can be satisfied using specific modified hybrid control algorithm developed from Direct-PWM, which will be discussed later. As labeled in the Fig. 1, from Stage 1 to Stage 6, the voltages of them are 6 kV, 6 kV, 6 kV, 6 kV, 4 kV and 2 kV, respectively. The sum of them is 30 kV.

The main characteristics of this design and the improvements compared with past designs are as following:

1) The peak value of the output voltage is ± 30 kV, and the minimum step of the waveform is 2 kV, so it is a 31-level converter. Compared with traditional two-level or three-level converters, the quality of the output waveform can be much better.
2) If in all the stages, only IGBTs are used, then the total number of stages required is 30/2=15. So the all-IGBT structure will be much more complex than this design.
3) If in all the stages, only IGCTs are used, obviously, by only using 5 stages will the 30 kV output be achieved. But without IGBT components, the maximum operation frequency of the whole converter cannot exceed 500 Hz, and then the quality of the output waveform will be much worse than this design.

So the use of IGCT and IGBT hybrid cascade structure takes the advantages of both IGCT and IGBT, and also eliminates their own disadvantages.

The operation conditions for each stage corresponding to different output voltage levels (The switching table) are summarized as in Table I.

TABLE I**:** THE SWITCHING TABLE

	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6
28~30 kV	ON: 6 kV	ON: 6 kV	ON: 6 kV	ON: 6 kV	ON: 4 kV	PWM: 0~2 kV
26~28 kV	ON: 6 kV	ON: 6 kV	ON: 6 kV	ON: 6 kV	ON: 4 kV	PWM: -2~0 kV
24~26 kV	ON: 6 kV	ON: 6 kV	ON: 6 kV	ON: 6 kV	OFF: 0 kV	PWM: 0~2 kV
22~24 kV	ON: 6 kV	ON: 6 kV	ON: 6 kV	OFF: 0 kV	ON: 4 kV	PWM: 0~2 kV
20~22 kV	ON: 6 kV	ON: 6 kV	ON: 6 kV	OFF: 0 kV	ON: 4 kV	PWM: -2~0 kV
18~20 kV	ON: 6 kV	ON: 6 kV	ON: 6 kV	OFF: 0 kV	OFF: 0 kV	PWM: 0~2 kV
16~18 kV	ON: 6 kV	ON: 6 kV	OFF: 0 kV	OFF: 0 kV	ON: 4 kV	PWM: 0~2 kV
14~16 kV	ON: 6 kV	ON: 6 kV	OFF: 0 kV	OFF: 0 kV	ON: 4 kV	PWM: -2~0 kV
12~14 kV	ON: 6 kV	ON: 6 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	PWM: 0~2 kV
10~12 kV	ON: 6 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	ON: 4 kV	PWM: 0~2 kV
8~10 kV	ON: 6 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	ON: 4 kV	PWM: -2~0 kV
6~8 kV	ON: 6 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	PWM: 0~2 kV
4~6 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	ON: 4 kV	PWM: 0~2 kV
2~4 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	ON: 4 kV	PWM: -2~0 kV
0~2 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	PWM: 0~2 kV
-2~0 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	PWM: -2~0 kV
-4~-2 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	ON: -4 kV	PWM: 0~2 kV
-6~-4 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	ON: -4 kV	PWM: -2~0 kV
-8~-6 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	ON: -6 kV	OFF: 0 kV	PWM: -2~0 kV
-10~-8 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	ON: -6 kV	ON: -4 kV	PWM: 0~2 kV
-12~-10 kV	OFF: 0 kV	OFF: 0 kV	OFF: 0 kV	ON: -6 kV	ON: -4 kV	PWM: -2~0 kV
-14~-12 kV	OFF: 0 kV	OFF: 0 kV	ON: -6 kV	ON: -6 kV	OFF: 0 kV	PWM: -2~0 kV
-16~-14 kV	OFF: 0 kV	OFF: 0 kV	ON: -6 kV	ON: -6 kV	ON: -4 kV	PWM: 0~2 kV
-18~-16 kV	OFF: 0 kV	OFF: 0 kV	ON: -6 kV	ON: -6 kV	ON: -4 kV	PWM: -2~0 kV
-20~-18 kV	OFF: 0 kV	ON: -6 kV	ON: -6 kV	ON: -6 kV	OFF: 0 kV	PWM: -2~0 kV
-22~-20 kV	OFF: 0 kV	ON: -6 kV	ON: -6 kV	ON: -6 kV	ON: -4 kV	PWM: 0~2 kV
-24~-22 kV	OFF: 0 kV	ON: -6 kV	ON: -6 kV	ON: -6 kV	ON: -4 kV	PWM: -2~0 kV
-26~-24 kV	ON: -6 kV	ON: -6 kV	ON: -6 kV	ON: -6 kV	OFF: 0 kV	PWM: -2~0 kV
-28~-26 kV	ON: -6 kV	ON: -6 kV	ON: -6 kV	ON: -6 kV	ON: -4 kV	PWM: 0~2 kV
-30~-28 kV	ON: -6 kV	ON: -6 kV	ON: -6 kV	ON: -6 kV	ON: -4 kV	PWM: -2~0 kV

III. CONTROL METHODS

To design a proper control method is a core task of this research. The target of the control of this converter is to enable the converter to give a correct output with good quality according to an artificial reference signal and to limit the operation frequencies of each switching components within their normal ranges.

A. Control Algorithm

The multilevel converter is controlled using hybrid Direct-PWM Method. In Direct-PWM Method, time is divided into a series of control periods, marked as T_S. Within each control period T_S, each stage is set to be ON/OFF during the whole T_S or set to be ON for a certain time period less than T_S, marked as T_{ON}. Stage 1~5 are built using IGCT components, whose working frequency is not so high as IGBT, so they are set to be ON or OFF during the whole T_S in order to limit the switching frequency. And Direct-PWM is applied to Stage 6 to give output voltage varying from -2 kV~2 kV in order to polish the shape of the overall output waveform.

Under normal operation, the reference signal can be assumed to be within -30 kV~30 kV. In order to realize the control method stated above, the control algorithm is designed as the control chart shown in Fig. 2 below. The following points are to be mentioned:

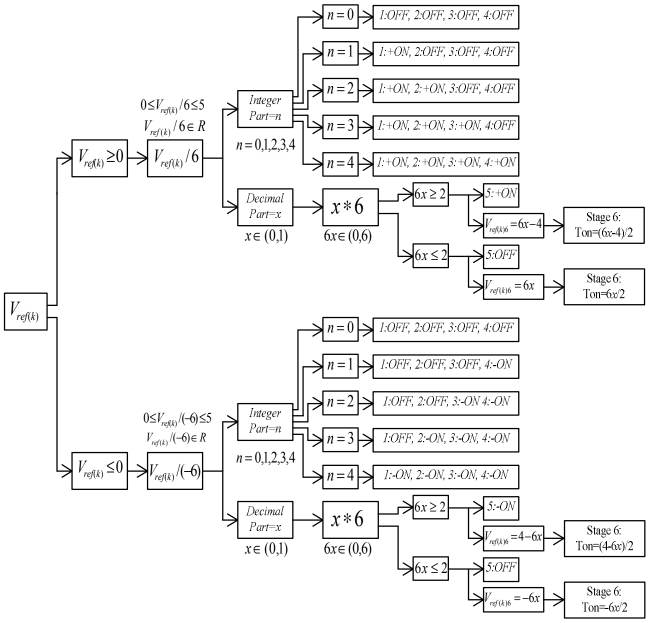

Figure 2: The diagram of control algorithm

1) First, the value of the reference signal is sampled at the beginning of each control period. This value is used for determining the ON/OFF status for Stages 1~5 during this control period and also for determining the switching direction and ON time for Stage 6 during this control period.
2) Then, determine the input reference signal to be positive or negative. Whether the reference signal is positive or negative determine the ON direction for each stage (For example, +ON means to output +6 kV and –ON means to output -6 kV).
3) The input reference signal is divided by 6, and the integer part *n* and decimal part *x* of the quotient is extracted respectively. The value of the integer part *n* means the number of 6 kV IGCT stages which need to be tuned ON during this control period T_S.
4) The decimal part *x* is multiplied by 6 and then used to determine the ON/OFF state for Stage 5. If *6x* is larger than 2 kV, then Stage 5 is set to be ON, and the different between *6x* and the output of Stage 5 (4 kV), which is *6x-4*, is then used as the reference signal for Stage 6 for generating Direct-PWM waveform; If *6x* is lower than 2 kV, then Stage 5 is set to be OFF, and *6x* is then used as the reference signal for Stage 6 for generating Direct-PWM waveform.
5) Positive and negative input reference signal share the same operation principle with only the ON direction different for Stage 1~5.

B. Direct-PWM for Stage 6

According to the above control chart, the ON/OFF status for Stages 1~5 and reference signal $V_{ref(k)6}$ is determined during one control period T_S. Using the above algorithm, the value of $V_{ref(k)6}$ always falls within the interval of [-2 kV, 2 kV].

Let the switching function for Stage 6 to be *S*. So *S* can be -2, 0 or 2. As in Fig. 3, $V_{ref(k)6}$ is the value of the reference signal sampled at time t_k, the beginning of one control period, T_S. In order to give and output of $V_{ref(k)6}$ by PWM, the ON time of this stage should be calculated according to equal-area principle, which means the two shaded areas should have the same value. By equalizing the two areas, we have

$$V_{ref(k)6} \cdot T_S = 0 \cdot T_{sOFF} + 2 \cdot T_{sON} \tag{1}$$

$$T_{sON} = \frac{V_{ref(k)6} \cdot T_s}{2} \tag{2}$$

where the value of $V_{ref(k)6}$ can be obtained using the algorithm illustrated in the above control chart [3, 8].

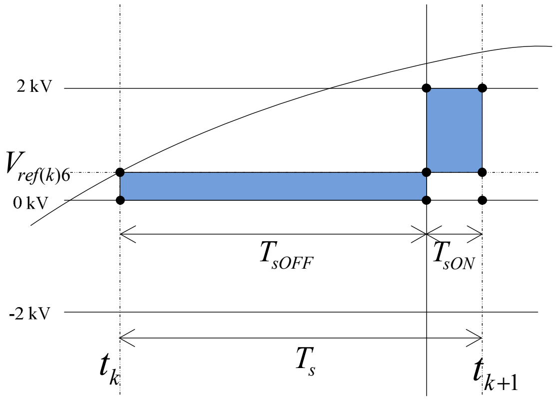

Figure 3: The calculation of T_{sON} during one control period

The ON time of Stage 6, T_{sON}, can be obtained by the above formula, but actually, this T_{sON} can be put into any place during T_S. It can be in the beginning of T_S, the end of T_S or in some intermediate place of T_S. For the minimizing of the switching frequency, this T_{sON} should be put either in the beginning or the end of T_S. And whether to put it in the beginning or the end is determined by the end status of the previous control period. The determination principle is illustrated as in Table II.

TABLE II: PRINCIPLE FOR DETERMINING THE PLACE TO PUT THE ON TIME DURING A CONTROL PERIOD T_S

		The ON direction of current control period	
		+ON	-ON
The status at the end of the previous control period	+ON	T_{sON} at the beginning of T_S	T_{sON} at the beginning of T_S
	OFF	T_{sON} at the end of T_S	T_{sON} at the end of T_S
	-ON	T_{sON} at the beginning of T_S	T_{sON} at the beginning of T_S

To illustrate the relationship between the PWM control of Stage 6 and ON/OFF control of Stage 5 (similar relationship with Stages 1~4), the operations of Stage 5 and Stage 6 during the first SIX control periods are analyzed. The value of the reference signal is sampled at the beginning of every control period. Assuming a sinusoidal reference signal, the sampling value corresponding to sampling time is in Table III below (The control frequency is set to be 5 kHz).

TABLE III: THE SAMPLED VALUES OF THE REFERENCE SIGNAL CORRESPONDING TO THE SAMPLING TIME

Time (s)	0	0.0002	0.0004	0.0006	0.0008	0.0010	0.0012
Sample (kV)	0	1.884	3.760	5.621	7.461	9.271	11.044

In Fig. 4, the waveform in the upper block is the output of Stage 5 and the waveform in the lower block is the output of Stage 6. The ON/OFF status and T_{sON}/T_S for Stage 6 at each control period will be analyzed one by one.

Control Period 1: At the beginning of Control Period 1, the sampled value of the reference signal is 0 kV. So Stage 5 keeps OFF and T_{sON} for Stage 6 is zero.

Control Period 2: At the beginning of Control Period 2, the sampled value of the reference signal is 1.884 kV, which is larger than 0 and lower than 2 kV. According to the control algorithm, Stages 1~4 and Stage 5 should keep OFF, and T_{sON}/T_S for Stage 6 should be 1.884/2=94.2%, in positive direction. And according to the principle in Table II, this ON-time should be put at the end of this control period.

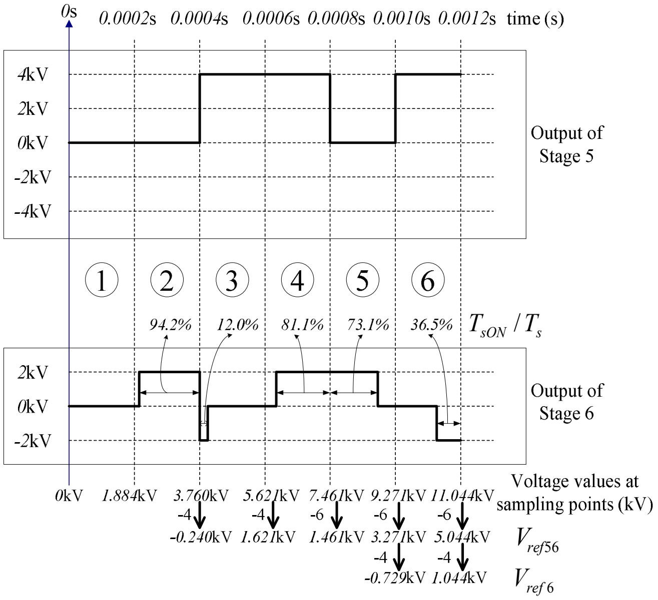

Figure 4: The ON/OFF and PWM status for Stage 5 and Stage 6 during the first SIX control periods

Control Period 3: At the beginning of Control Period 3, the sampled value of the reference signal is 3.760 kV, which is larger than 2 and lower than 6 kV. According to the control algorithm, Stages 1~4 should keep OFF and Stage 5 should be ON in positive direction. When Stage 5 gives a 4 kV output, the reference signal for Stage 6 then becomes 3.760-4=-0.24 kV. So T_{sON}/T_S for Stage 6 should be 0.24/2=12%, in negative direction. And according to the principle in Table II, this ON-time should be put at the beginning of this control period.

Control Period 4: At the beginning of Control Period 4, the sampled value of the reference signal is 5.621 kV, which is larger than 2 and lower than 6 kV. According to the control algorithm, Stages 1~4 should keep OFF and Stage 5 should be ON in positive direction. When Stage 5 gives a 4 kV output, the reference signal for Stage 6 then becomes 5.621-

4=1.621 kV, so T_{sON}/T_S for Stage 6 should be 1.621/2=81.1%, in positive direction. And according to the principle in Table II, this ON-time should be put at the end of this control period.

Control Period 5: At the beginning of Control Period 5, the sampled value of the reference signal is 7.461 kV, which is larger than 6 and lower than 12 kV. According to the control algorithm, Stage 1 should be ON in positive direction (Stages 2~4 still OFF), which gives a 6 kV output. So the reference signal for Stage 5, V_{ref56} is then 7.461-6=1.461 kV. So Stage 5 should be OFF, and T_{sON}/T_S for Stage 6 should be 1.461/2=73.1%, in positive direction. And according to the principle in Table II, this ON-time should be put at the beginning of this control period.

Control Period 6: At the beginning of Control Period 6, the sampled value of the reference signal is 9.271 kV, which is larger than 6 and lower than 12 kV. According to the control algorithm, Stage 1 should be ON in positive direction (Stages 2~4 still OFF), which gives a 6 kV output. So the reference signal for Stage 5, V_{ref56} is then 9.271-6=3.271 kV. This time it is the same as Control Period 3, Stage 5 should be ON in positive direction and gives 4 kV output so that the reference signal for Stage 6 is 3.271-4=0.729 kV, so T_{sON}/T_S for Stage 6 should be 0.729/2=36.5%, in negative direction. And according to the principle in Table II, this ON-time should be put at the end of this control period.

The control method afterwards is similar to the first SIX typical control periods. And one thing to be noticed is that in Control Period 4 and 5, the two T_{sON} are connected together so that during the two control periods, Stage 6 only turns ON and OFF once. So the switching frequencies of the switching components can be lowered down by large scale according to the principle in Table II.

IV. SIMULATION AND EXPERIMENT RESULTS

To verify the practicability of the proposed structure and control methods, some simulations are carried out using PSCAD. The simulation model is developed on the topology shown in Fig. 1. The parameters for simulation are shown in Table IV.

TABLE IV: THE PARAMETERS FOR THE SIMULATION

Reference Signal	30 kV_{peak}, 50 Hz, Sinusoidal wave
Sampling Frequency	5 kHz
DC link Capacitance	5 mF per each bridge
Output Filter	No filter

The waveforms of the reference signal (upper) and the output signal (lower) are shown in Fig. 5.

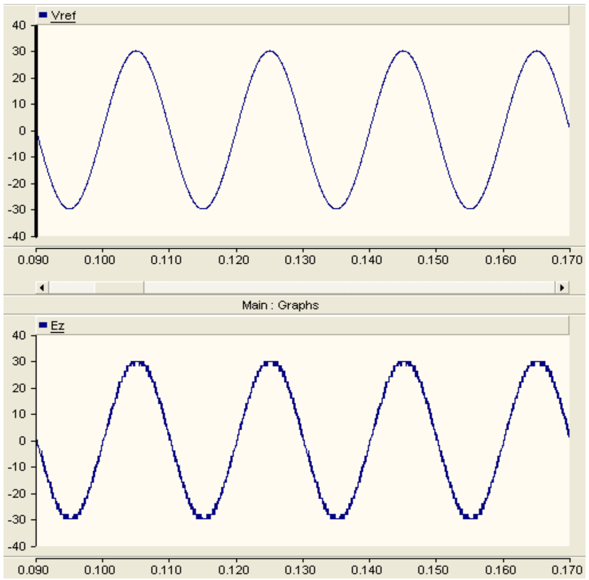

Figure 5: The waveforms of the reference signal (upper) and the output signal (lower)

The THD of the output waveform is 0.168%, and the measured operation frequencies of each switching components are shown in Table V.

TABLE V: THE MEASURED SWITCHING FREQUENCY OF EVERY SWITCHING COMPONENT

Stage and Switch	Switching Frequency (Hz)
Stage 1 (6 kV, IGCT) G11, G12, G13, G14	100
Stage 2 (6 kV, IGCT) G21, G22, G23, G24	100
Stage 3 (6 kV, IGCT) G31, G32, G33, G34	100
Stage 4 (6 kV, IGCT) G41, G42, G43, G44	100
Stage 5 (4 kV, IGCT) G51, G52, G53, G54	500
Stage 6 (2 kV, IGBT) G61, G62, G63, G64	4500

If the voltage of the reference signal is changed to 12 kV (for the comparison with the hardware test) and 3 kV, the THDs of the output waveforms are 0.765% and 2.772%, respectively. These THD values are much lower than the performances of traditional power converters. From the simulation result, it is seen that the converter can give correct output according to the reference signal and the operation frequencies of each switching component is within its normal range.

An experiment prototype is also built for the verification of this hybrid structure and hybrid control algorithm. The hardware only contains the last three stages and the experiment voltage is 1/100 of the original design for the practicability and safety of laboratory use. Actually the last three stages can fully represent the whole control algorithm and structure, and the first several IGCT stages are just a simple expansion of the last three core stages.

The reference signal of for the experiment is a sinusoidal wave of 120 V_{peak}(84.85 V_{rms}), 50 Hz. The output waveform of the multilevel converter and its harmonic spectrum are shown in Fig.6. The THD of the output waveform is 10.6%. Although this value is larger than the simulation result due to experiment errors, this parameter is much better than traditional converters.

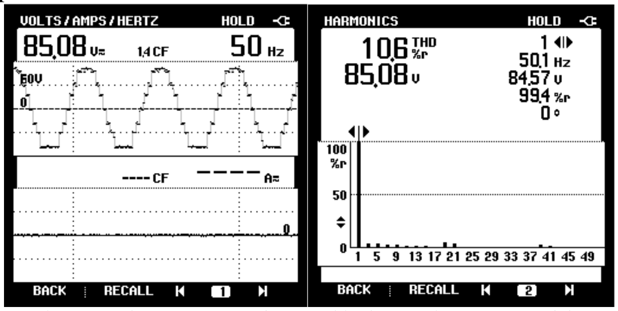

Figure 6: The output waveform and its harmonic spectrum of the multilevel converter for a sinusoidal reference signal

V. CONCLUSIONS

In this paper, a novel multilevel converter using IGCT and IGBT hybrid cascaded structure is proposed based on the requirement for medium-voltage large-capacitance applications (RPC for example). By using only 6-stage cascaded structure, the output voltage can reach 30 kV so that it can be directly connected to the traction power system without any linking transformer. And the output THD of it is much better than traditional designs. For the proposed structure, a hybrid control method is designed so as the proposed converter can give a correct output waveform according to an artificial reference signal and the operation frequencies of each switching component are kept within their normal range.

The design is then verified by PSCAD simulation, and the results verified the correctness and practicability of the design and also proved that the designed hybrid control method can keep the operation frequencies of the high voltage stages within the normal operation range of IGCT ($\leq 500Hz$). A hardware prototype of the representative three stages is also constructed and tested based on theoretical design and simulation. Both the simulation and experiment results showed that the design of the new multilevel converter is successful and it fulfills the main target of the design, which is to enable the power converter (RPC) to be directly connected to the traction power system without linking transformer.

REFERENCES

[1] JianZheng, "A Study on STATCOM based on Hybrid Cascaded Multilevel Inverters", Master of Engineering Thesis of Nanjing University of Science and Technology, 2009.06, retrieved from Wanfang Data

[2] Wei Yingdong, "Research on Control of Comprehensive Compensation for Traction Substations based on the STATCOM Technology", PhD Thesis of Tsinghua University, 2009.10, retrieved from Wanfang Data

[3] Longhua Zhou, Qing Fu, Xiangfeng Li and Changshu Liu, "A Novel Multilevel Power Quality Compensator for Electrified Railway", Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International

[4] Zhuo Sun, Xinjian Jiang, Dongqi Zhu, and Guixin Zhang, "A novel Active Power Quality Compensator Topology for Electrified Railway", IEEE Transactions on power electronics, Vol. 19, No. 4, July 2004

[5] Tetsuo UZUKA, Shouji IKEDO, "Railway Static Power Conditioner Field Test", Power Electronics Conference (IPEC), 2010 International

[6] Kießling,Puschmann, Schmieder, „Fahrleitungen elektrischer Bahnen - Planung, Berechnung, Ausführung", SIEMENS, 2008.4

[7] Fang Z. Peng, "A Generalized Multilevel Inverter Topology with Self Voltage Balancing", 2001, Industry Applications, IEEE Transactions on Volume: 37 , Issue: 2

[8] Yuanhua Chen, "Investigation of Control Strategies for Hybrid Multilevel Inverter", PhD Thesis of Tsinghua University, 2003.10, retrieved from Wanfang Data

[9] XiaomingQuan, "A Study on the Control Technology of Cascaded Multilevel Inverters", Master of Engineering Thesis of Zhongnan University, 2009.05, retrieved from Wanfang Data

[10] Mohan, Undeland, Robbins, "Power Electronics-Converters, Applications, And Design", Third Edition, Wiley, 2008.10