Per-Unit Design of a Transformerless, H-Bridge Dynamic Voltage Restorer with Closed-Loop Load Voltage and Current-Mode Control

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***Abstract*—Based on the modeling of a transformerless, H-bridge, double control loops Dynamic Voltage Restorer (DVR), its stability, harmonics compensation capability, load adaptability and response time are both investigated and analyzed in per-unit system, which demonstrate and predict a stable and good compensating feature. Using the per-unit system to design, those system parameters can be applied to other capacity and base voltage systems conveniently and also in a more general manner than the physical unit system. The determination of DVR capacity and the corresponding DC storage capacitance and rating required is also discussed. This research work can also act as a design reference for constructing different capacities transformerless, H-bridge double loops control DVR from 1kVA to 100kVA. Finally, simulation and experimental results are presented to validate the per-unit design method and demonstrate its good system performance.**

Keywords-Dynamic Voltage Restorer (DVR), power quality

NOMENCLATURE

" ^ "	*Peak of the associates waveform*
A_t	*Triangle carrier*
u_{dc}	*DC bus voltage*
L	*Filtering inductor*
C	*Filtering capacitor*
α	*Filtering capacitor current gain*
β	*Load voltage feedback gain*
K_v	*Proportional gain in PI controller*
τ	*Time constant in PI controller*
K_T	*Voltage transducer gain*
K_{Tri}	*Triangular wave voltage gain,* $K_{Tri} = \frac{1}{\hat{A}_t}$
K_m	*Fundamental inverter gain when* $\hat{A}_t = 1$
" _ "	*Bar under the variables represents the corresponding per-unit value*

I. INTRODUCTION

With the prolific use of power electronic devices and nonlinear power electronic loads in power system, it seriously deteriorates the power quality in the electricity utilization system. Also, when some power faults appear either at power transmission or distribution level, transient voltage sags or swells always result [1]. For some modern high-tech voltage-sensitive load equipments such as: automatic production line, high precision processing industry, computer system, etc., this has made production, industrial processes and data processing much more vulnerable to degradation in the quality of power supply. Voltage quality problems in the form of deep voltage sag, three-phase unbalance, and long swell duration can cause severe process disruptions, which result in substantial economic and data losses [2], [3]. Clearly, there is a need, from both utilities and customers for power quality improvement.

Thus the introduction of the Dynamic Voltage Restorer (DVR) is a welcome development as the device to compensate the voltage quality problems. DVR is a power electronic converter based device; designed to protect critical loads from the supply-side voltage disturbances. And it is capable of generating or absorbing real and reactive power at its ac terminals. The basic principle of a DVR is simple: by inserting a voltage of desired magnitude and frequency, in order to restore the load-side voltage balanced and sinusoidal [4], [5].

When DVR is implemented in a low voltage level distribution network, transformerless structure is usually better than the conventional transformer one by eliminating the transformer phase shift, voltage drop, harmonics loss, bulky size, expensive cost and the problems of saturation and inrush currents associated with the transformer magnetization phenomenon [6]. However, a transformerless DVR is indispensable to use the circuit configuration in Fig. 1: three H-bridge inverters with separated DC-links configuration. Otherwise, if common DC-link configuration is implemented, overlapped conduction period caused by switches will subject to short-circuit scenario. Installation of a diode rectifier circuit to support transformerless DVR provides an economical way for the DC-link to negotiate active power, which can reduce the DC-link voltage fluctuation, and provide stable storage energy for voltage compensation.

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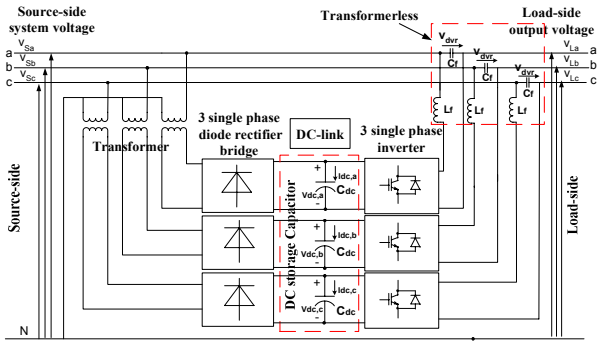

Fig. 1. A diode rectifier supported transformerless DVR

At the very beginning, the voltage quality compensator makes use of feedforward control method [7], [8]. Even though the feedforward control method has the advantages of simple implementation and fast dynamic response, it can not eliminate the load current effect on the compensation result. Moreover, the feedforward control shows large voltage overshoot and inaccurate regulation of the output voltage owing to the voltage drop across the series impedance and the filter [9]. Due to these problems, a combination of feedforward and feedback control method is proposed [8], the addition of feedback control can significant improve the compensation result. However, this method still cannot solve the adaptability problem of nonlinear load, because the level of damping deteriorates as the load power factor decreases. In [10], a closed-loop load voltage and current mode double feedback loops control method has been proposed, it can enhance the DVR tracking ability, provide better voltage regulation and improve the poor damping problem existed in the feedforward control. As a result, a transformerless, H-bridge structure with closed-loop load voltage and current mode control strategy could be a good combination for the design of a low voltage level DVR system.

In power system or distribution power system analysis, it is usually convenient to apply per-unit system to normalize system variables. Comparing to the use of physical units (amperes, volts, ohms, etc.), the per-unit system offers computational simplicity and a more general concept by eliminating units and expressing system quantities as dimensionless ratios. So in the following design analysis, the per-unit system is chosen so that those system parameters can also be applied to other capacity and base voltage systems. Finally, the effectiveness of the per-unit designed transformerless, H-bridge DVR with double loops controlled system is illustrated based on the simulation and experimental results presented in sections IV.

II. Modeling of ATransfomerless, H-Brdige DVR with Double Loops Control

With the inverter model equivalents as a gain K_m equals to DC bus voltage u_{dc}, which is linear, the block diagram model of a transformerless, H-bridge DVR with double loops control can be shown in Fig. 2 [11]. From Fig. 2,

$$u_o(s) = G_{cr}(s)u_r(s) + G_{csys}(s)u_{sys}(s) + G_{ci}(s)i_l(s) \quad (1)$$

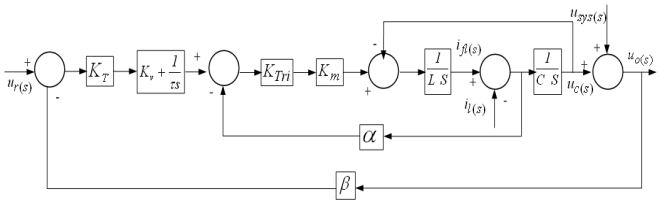

Fig. 2. System block diagram model of this transformerless DVR

where G_{cr} is the closed-loop transfer function between the reference signal u_r and the load output voltage u_o, G_{csys} is the closed-loop transfer function between the system input voltage u_{sys} and load output voltage u_o, and G_{ci} is the closed-loop transfer function between the load current i_l and the load output voltage u_o respectively.

$$G_{cr}(s) = \frac{K_T K_{Tri} K_m (1 + K_v \varpi)}{LC\varpi^3 + K_{Tri}K_m C\alpha\varpi^2 + \varpi(1 + K_T K_{Tri} K_m K_v \beta) + K_T K_{Tri} K_m \beta} \quad (2)$$

$$G_{csys}(s) = \frac{\varpi(LCs^2 + 1 + K_{Tri}K_m C\alpha s)}{LC\varpi^3 + K_{Tri}K_m C\alpha\varpi^2 + \varpi(1 + K_T K_{Tri} K_m K_v \beta) + K_T K_{Tri} K_m \beta} \quad (3)$$

$$G_{ci}(s) = \frac{-L\varpi^2}{LC\varpi^3 + K_m K_{Tri} C\alpha\varpi^2 + \varpi(1 + K_m K_T K_{Tri} K_v \beta) + K_m K_T K_{Tri} \beta} \quad (4)$$

Based on the system block diagram model in Fig. 2 and (1)-(4), the detail of system performances including DVR stability, voltage harmonics compensation capability, load adaptability and response time can be discussed and analyzed in the following section.

III. Investigation of DVR System Performances

A. Stability Study

According to Fig. 2, the open-loop transfer function G_{or} between u_o and u_r :

$$G_{or}(s) = \frac{K_T K_{Tri} K_m (1 + K_v \varpi)}{\varpi\left(LCs^2 + K_{Tri} K_m C\alpha s + 1\right)} \quad (5)$$

With one zero and three poles:

$$S_{oz} = -\frac{1}{K_v \tau} \quad (6)$$

$$S_{op1} = 0,\ S_{op2,3} = -\frac{\alpha K_{Tri} K_m}{2L} \pm \sqrt{\left(\frac{\alpha K_{Tri} K_m}{2L}\right)^2 - \frac{1}{LC}} \quad (7)$$

From (7), S_{op2} and S_{op3} both have negative real part, which is located in the left s-plane. By changing the system parameter values, the locations of S_{op2} and S_{op3} will change accordingly.

If $\left(\frac{\alpha K_{Tri} K_m}{2L}\right)^2 < \frac{1}{LC}$, the system has a pair of complex poles.

$$S_{op2,3} = -\frac{\alpha K_{Tri} K_m}{2L} \pm j\sqrt{-\left(\frac{\alpha K_{Tri} K_m}{2L}\right)^2 + \frac{1}{LC}} \quad (8)$$

If $(\frac{\alpha K_{Tri}K_m}{2L})^2 \geq \frac{1}{LC}$, the system has two negative real roots.

$$S_{op2,3} = -\frac{\alpha K_{Tri}K_m}{2L} \pm \sqrt{(\frac{\alpha K_{Tri}K_m}{2L})^2 - \frac{1}{LC}} \quad (9)$$

When the root locus gain approaches to infinite, there are also two root locus approaches infinite. Moreover, the slope of two asymptotes (10) is $\pi/2$ and $3\pi/2$ and the intersection point between the two asymptotes and real-axis is σ_a, which can be calculated by (11):

$$\varphi_a = \frac{(2k+1)\pi}{n-m}(k = 0,1..., n-m-1) \quad (10)$$

where n= number of finite poles, m = number of finite zeros.

$$\sigma_a = \frac{\sum_{i=1}^{3} S_{opi} - \sum_{j=1}^{1} S_{ozj}}{2} = -\frac{1}{2}\left(\frac{\alpha K_{Tri}K_m}{L} - \frac{1}{K_v\tau}\right) \quad (11)$$

Selecting suitable system parameters can guarantee σ_a far away from the jω axis, and maintain a good system stability margin.

According to Fig. 2 and (2), by ROUTH-HURWITZ criterion, the Routh table can be obtained as follows:

s^3	$LC\tau$	$\tau(1+K_TK_{Tri}K_mK_v\beta)$
s^2	$K_{Tri}K_mC\alpha\tau$	$K_TK_{Tri}K_m\beta$
s^1	$\frac{\alpha CK_{Tri}K_m\tau^2(1+\beta K_{Tri}K_mK_TK_v)}{\alpha CK_{Tri}K_m\tau}$	
	$-\frac{CL\tau\beta K_{Tri}K_mK_T}{\alpha CK_{Tri}K_m\tau}$	
s^0	$K_TK_{Tri}K_m\beta$	

The closed loop system is stable if and only if there are no sign changes in the first column of the above table. Thus the system must fulfill the following four conditions:

Condition 1: $LC\tau > 0$ (12a)

Condition 2: $K_{Tri}K_mC\alpha\tau > 0$ (12b)

Condition 3:

$$\frac{\alpha CK_{Tri}K_m\tau^2(1+\beta K_{Tri}K_mK_TK_v) - CL\tau\beta K_{Tri}K_mK_T}{\alpha CK_{Tri}K_m\tau} > 0 \quad (12c)$$

Condition 4: $K_TK_{Tri}K_m\beta > 0$ (12d)

In order for the DVR system to have good stability, its system parameters should be designed so that $\frac{\alpha K_{Tri}K_m}{L} >> \frac{1}{K_v\tau}$ (11), and condition (12) are satisfied. Moreover, with the help of root locus and bode plot analysis, they can give more detail about the degree of system stability.

Assume the DVR capacity=10kVA and the capacity of the load in each phase = 3.3kVA, and the system frequency f = 50Hz. Table I shows system parameter quantities in base value.

TABLE I. SYSTEM PARAMETER QUANTITIES IN BASE VALUE

Quantities	Base Value
Voltage V_{base}	220V
Current I_{base}	15A
Impedance Z_{base}	14.67 V/A
Admittance Y_{base}	0.068 A/V
Angular Frequency $\omega_{base} = 2\pi f$	314.16 rad/s
Time base= $\frac{1}{\omega_{base}}$	3.18×10^{-3} s/rad

TABLE II. MODIFICATION OF SYSTEM PARAMETERS BETWEEN PHYSICAL UNIT TO PER-UNIT SYSTEM

System Parameters Physical unit ⇔ Per-Unit	System Parameters Physical unit ⇔ Per-Unit
$\underline{L} = L\times\frac{2\pi\times50}{Z_{base}}$	$\underline{K_{Tri}} = \frac{1}{\hat{A}_t}$
$\underline{C} = C\times\frac{2\pi\times50}{Y_{base}}$	$\underline{K_v} = K_v$
$\underline{\alpha} = \alpha\times I_{base}$	$\underline{K_T} = K_T\times V_{base}$
$\underline{\beta} = \beta$	$\underline{\tau} = \frac{\tau}{Time_{base}}$
$\underline{K_m} = \frac{u_{dc}}{V_{base}}$	$\underline{R} = \frac{R}{Z_{base}}$

TABLE III. A SET OF SYSTEM PARAMETERS IN PER-UNIT

System Parameters	Unstable Per-Unit Values (p.u.)	Stable Per-Unit Values (p.u.)
$\underline{Z_L}(\underline{L})$	0.75	0.163
$\underline{Y_C}(\underline{C})$	0.051	0.051
$\underline{\alpha}$	15	396
$\underline{\beta}$	1	1
$\underline{K_m}$	1.36	1.36
$\underline{K_{Tri}}$	0.083	0.083
$\underline{K_v}$	2	15
$\underline{K_T}$	21.04	21.04
$\underline{\tau}$	0.157	0.63

According to Table I, the per-unit system of the DVR system can be built by (13),

$$Quantity\ in\ Per\text{-}unit = \frac{Actual\ quantity}{Base\ value\ of\ quantity} \quad (13)$$

Table II shows the modification of the system parameters between physical unit system and per-unit system. And Table III shows a set of stable and unstable system parameters in per-unit format, which can be used to analyze the system typically.

In per-unit system, $\omega_{base} = 2\pi f$, $\underline{\omega} = \frac{\omega_{actual}}{\omega_{base}}$ so $\underline{\omega} = 1$, therefore $\underline{Z_L} = \underline{L}$ and $\underline{Y_C} = \underline{C}$.

Under the stable per-unit system parameters shown in Table III, the system has two negative real poles, and the two asymptotes intersect at a common point on the real axis of σ_a = -137.1 p.u. or -4.31× 104 rad/s (11), which guarantees the root locus in the left s-plane. Moreover, condition (12) is satisfied, thus the system is inherently stable.

According to the closed-loop transfer function (1), Fig. 3a shows the root locus diagram of the system under the stable per-unit parameters mentioned in Table III. From Fig. 3a, the zero and the three poles S_{cz}, S_{cp1}, S_{cp2}, S_{cp3} values are -0.106 p.u., -0.104 p.u., -17 p.u. and -257 p.u. or -33.3 rad/s, -32.6 rad/s, -5.34× 103 rad/s and -8.07× 104 rad/s, which all poles are located in the left s-plane. Using σ_a to express the intersection point between the asymptotic and real-axis, which is located between the two poles S_{cp2}, S_{cp3}. If the open-loop gain increases, the closed-loop poles will change according $S_{cp3} \to \sigma_a \to +\infty$ and $S_{cp2} \to \sigma_a \to -\infty$ respectively, but the position of the pole S_{cp1} does not vary a lot.

Fig. 3a also shows the bode diagram of the open-loop system. From open-loop bode diagram, the system is stable because it has a rather large stability margin of gain margin

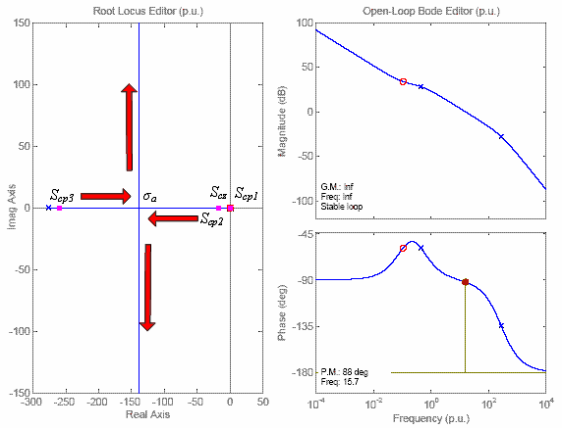

Fig. 3a. Root locus diagram and bode plot of the open loop system under stable per-unit values

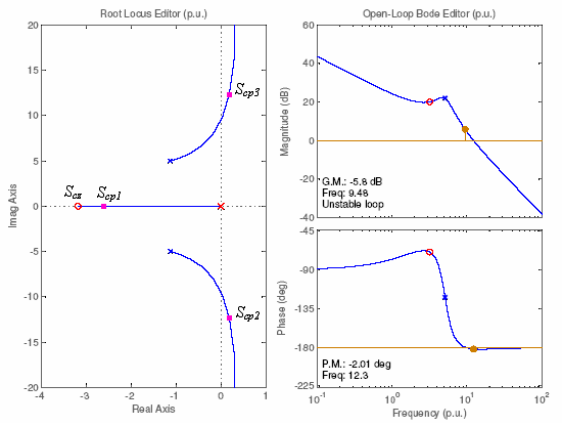

Fig. 3b. Root locus diagram and bode plot of the open loop system under unstable per-unit values

G.M.=inf dB, phase margin P.M.=88.0°. According to block diagram model in Fig. 2, if the DVR system is designed according those stable per-unit parameters shown in Table III, the DVR system will be always stable.

However, if the DVR system is designed according those unstable per-unit parameters shown in Table III, from Fig. 3b, the zero and the three poles S_{cz}, S_{cp1}, S_{cp2}, S_{cp3} values are -3.18 p.u., -2.61 p.u., (0.179+12.3i) p.u. and (0.179-12.3i) p.u. or -999.0 rad/s, -820.0 rad/s, (56.2+3.86× 10^3) rad/s and (56.2-3.86× 10^3) rad/s, which poles S_{cp2} and S_{cp3} are located in the right s-plane, where condition (12) does not satisfy. Moreover, Fig. 3b also shows an unstable bode diagram of the open-loop system, because it has a negative gain margin G.M.=-5.8 dB and phase margin P.M.=-2.01°. According to block diagram model in Fig. 2, if the DVR system is designed according those unstable per-unit parameters shown in Table III, the DVR system will be unstable.

B. Voltage Harmonics Compensation Capability

From Fig. 2, if treating the system input voltage u_{sys} as the closed-loop system disturbance, it will be desirable for u_o to track its reference signal value u_r only, and u_o should be normally unaffected by u_{sys} at least over a specified frequency range. Thus, the most preferable closed-loop gain G_{csys} is zero.

According to the closed-loop transfer function (3), Fig. 4 shows the bode diagram of u_o with respect to u_{sys} under the stable per-unit system parameters shown in Table III. From Fig. 4, the load output voltage u_o has large attenuation at low frequency band (about -22 dB at the fundamental frequency), which is preferable because u_{sys} is treating as the system disturbance. When it reaches at a high frequency of 2kHz, u_o is almost equal to u_{sys}. That means DVR cannot eliminate very high voltage harmonic components.

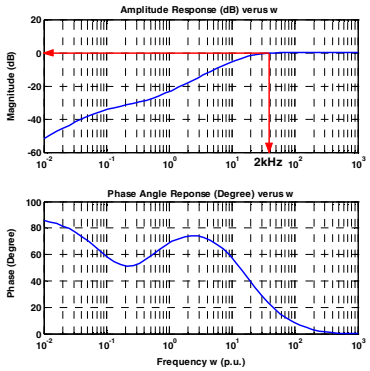

Fig. 4. Bode diagram of the closed-loop load output voltage with respect to the system input voltage under stable per-unit parameters

C. Load Adaptability

In order to enhance the load adaptability, it is better to have the load output voltage unaffected by the load current. From

Fig. 2, if treating the load current i_l as another disturbance similar as the system voltage u_{sys}, the most preferable closed-loop gain G_{ci} is also zero. Thus the system parameters should be designed so that the gain G_{ci} is small at all frequency range. If the closed-loop gain G_{ci} as in (4) is small at all frequency range, the DVR system can be claimed to have good load adaptability. When the switching frequency increases, smaller filter parameters and time constant τ can be used, this results in a better load adaptability. Within an acceptable range of the system losses and permitted operation range of the switching devices, increasing the switching frequency can enhance the system load adaptability.

This gain G_{ci} expresses the effect of the load current to the load output voltage and the bode-diagram under the stable per-unit values in Table III is shown in Fig. 5. At the fundamental frequency of $\underline{\omega = 1}$, the gain G_{ci} has an attenuation of about 35 dB, thus the current will not affect the load output voltage much, and this result can enhance the load adaptability. The resonance frequency point of the *LC* filter:

$$\underline{\omega_{resonance}} = \frac{1}{\sqrt{LC}} = 1\,1 p.u.$$

From Fig. 5, even at the resonance point of the *LC* filter, there does not contain an unstable or large harmonic resonance amplification phenomenon in the system. Therefore, the nonlinear load current will not cause an unstable output voltage. Therefore, the DVR system will contain good load adaptability.

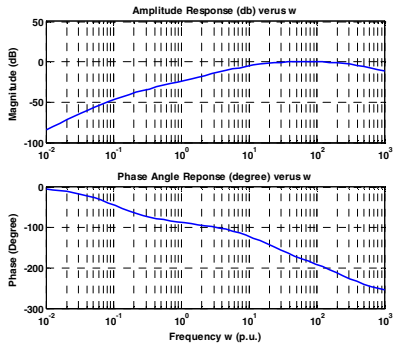

Fig. 5. Bode diagram of the closed-loop load output voltage with respect to the load current under stable per-unit parameters

D. Response Time

Lastly, the system parameter effect on the DVR response time will be discussed. By selecting system parameters appropriately, the DVR response time can be reduced. However, this action will usually decrease the system stability margin at the same time. Therefore, the response time and stability is always a trade-off relationship. The response speed can be investigated by applying a step input $u_r(s) = \frac{1}{s}$ to (2):

$$u_o(s) = \frac{K_T K_{Tri} K_m (1 + K_v \varpi)}{LC\varpi^3 + \alpha C K_{Tri} K_m \varpi^2 + (1 + \beta K_v K_{Tri} K_m K_T)\varpi + \beta K_{Tri} K_m K_T} \times \frac{1}{s} \quad (14)$$

Under the stable per-unit system parameters mentioned in Table III, Fig. 6 shows that the DVR will have a fast response when a step input is applied to it. The load output voltage requires about 0.2 p.u. to track the reference voltage, with less steady state error.

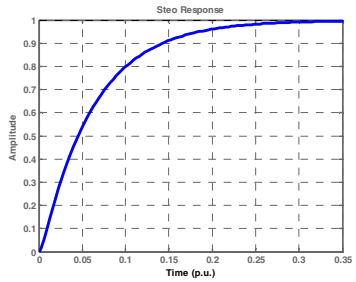

Fig. 6. Response time study of the DVR

Therefore, if the DVR system parameters are designed according to the stable per-unit values in Table III, it will have a stable, fast response with less steady state error. Moreover, it has rather good load adaptability and voltage harmonics compensation capability.

E. Capacity & DC Storage Capacitor Determination of DVR System

1) DVR Capacity Determination

Since the filtering capacitor *C* is series connected between the system side and load side, and the impedance of the filtering capacitor *C* is always large comparing with the filtering inductor *L* and IGBTs, this forces most of the system current passing to the load side through the IGBTs, shown in Fig. 7. As a result, the system support load rating will be limited by the DVR capacity. The maximum load rating in each phase will be one-third of the DVR capacity. In other words, the ratio between the transformerless DVR capacity and its support load rating in each phase = 3:1. Once the maximum load rating of a building or area is given, the minimum capacity of the DVR system required can be known.

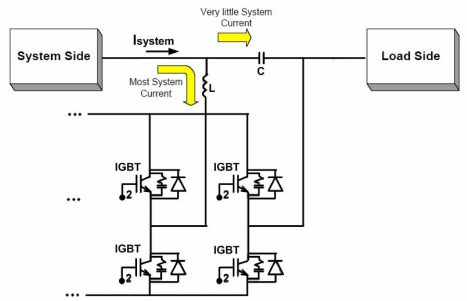

Fig. 7. Diagram of system current flows

2) DC Storage Capacitor Determination

The DC storage capacitance can be designed though (15), it aims to keep the DC link voltage in an acceptable fluctuant situation. The voltage fluctuation of the DC capacitor can be described by:

$$\Delta u_{dc} = \left| \frac{1}{C_{dc}} \int_{T/2}^{T} \sqrt{2} I_m \sin \omega t dt \right| \quad (15a)$$

$$C_{dc} = \frac{2\sqrt{2}I_m}{\omega \Delta u_{dc}} \quad (15b)$$

,where T is the fundamental period, C_{dc} represents the DC storage capacitance, I_m represents the nominal rated current, and Δu_{dc} is the DC bus allowable fluctuation voltage level. From (15), the design of the minimum DC storage capacitance required can be found.

Considering the fundamental component only, the DVR energy absorption during swell is:

$$\int_{t_0}^{t} p_{dc}(\tau)\, d\tau = \int_{t_0}^{t} (P_{in} - P_{out})\, d\tau \quad (16)$$

, p_{dc} is the DC capacitor absorbed power, $P_{in} = |V_{sys1}||I_{L1}|cos(\varphi_1)$ represents the fundamental system input power, $P_{out} = |V_{o1}||I_{L1}|cos(\varphi_1)$ represents the fundamental load output power, subscript "*1*" represents the fundamental component, fundamental load power factor= fundamental system input power factor= $cos(\varphi_1)$, V_{sys1} and V_{o1} represent the fundamental system input and load output voltage, I_{L1} represents the fundamental load current.

The stored energy increase will raise the DC-link voltage level, which the relationship between capacitor stored energy and voltage level can be represented by (17),

$$\int_{t_0}^{t} p_{dc}(\tau)\, d\tau < \frac{C_{dc}}{2}\left[v_{dc\,max}^2 - V_{dc0}^2\right] \quad (17)$$

, $v_{dc\,max}$ represents the permitted maximum DC capacitor voltage, V_{dc0} represents the DC capacitor initial voltage and V_{dc0} =1.35× nominal rated voltage, 1.35 is the diode rectifier bridge ratio. For safety operation, the energy absorbed must not charge the DC storage capacitor voltage over its maximum rating (17).

From (16) and (17) yields (18),

$$(|V_{sys1}| - |V_{o1}|) \times |I_{L1}| \times (cos(\varphi_1) \times \Delta t') < \frac{C_{dc}}{2}\left[v_{dc\,max}^2 - (1.35|V_{o1}|)^2\right] \quad (18)$$

,where $\Delta t' = t - t_0$ is the summation of DVR response time and calculation time of voltage swell compensation algorithm [12]. In that duration time $\Delta t'$, the DVR will absorb active power unavoidably and thus raise the DC-link voltage level until the DVR response and perform voltage swell compensation.

Assume the worst case for a voltage swell situation happens.

Set $\underline{|V_{o1}|}$, $\underline{|I_{L1}|}$= nominal rated voltage and current magnitude = 1 p.u.

System swell voltage magnitude $\underline{|V_{sys1}|}$ = 1.5 p.u.

Fundamental load power factor $cos(\varphi_1)$ =1 (pure resistive)

Substitute the above data into (18) yields (19),

$$\underline{v_{dc\,max}} > \sqrt{\frac{\Delta t'}{\underline{C_{dc}}} + 1.8225} \quad (19)$$

As a result, based on (15) and (19), the capacitance and rating of the storage capacitor respect to different degrees and time durations of voltage sag and swell compensation in any DVR capacity can be designed.

IV. Simulation & Experimental Results

A. *Simulation Results on a 1kVA, 10kVA and 100kVA DVR Model*

Based on the stable and unstable per-unit system parameters in Table III and DC storage capacitor determination in previous section, the simulation results on a 1kVA, 10kVA and 100kVA DVR model can be shown in Fig. 8 – Fig. 11 respectively, where the Table III corresponding system parameters in physical unit are shown in Table IV.

TABLE IV. A Set of System Parameters in Physical Unit

DVR System Parameters	1kVA	Unstable 10kVA	10kVA	100kVA
L	76mH	35mH	7.6mH	0.76mH
C	1.1μF	11μF	11μF	110μF
α	26.4	15	26.4	26.4
β	1	1	1	1
K_m	300	300	300	300
K_{Tri}	0.083	0.083	0.083	0.083
K_v	15	2	15	15
K_T	0.09565	0.09565	0.09565	0.09565
τ	2ms	0.5ms	2ms	2ms

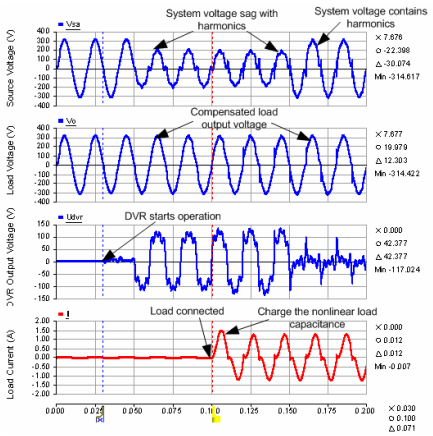

Fig. 8. Simulation results of a stable 1kVA DVR system

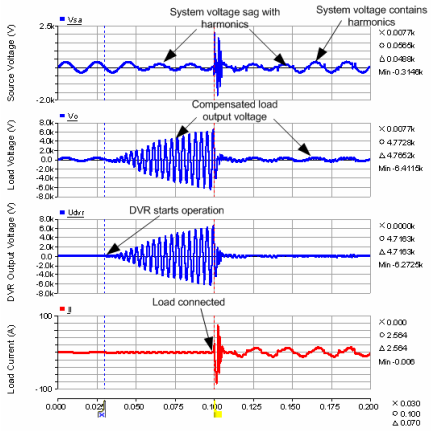

Fig. 9. Simulation results of an unstable 10kVA DVR system

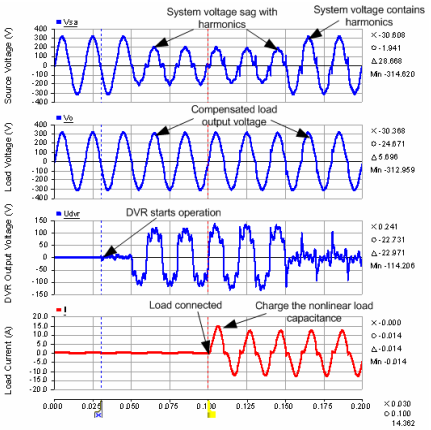

Fig. 10. Simulation results of a stable 10kVA DVR system

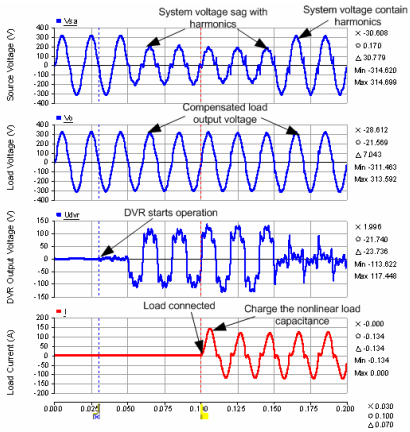

Fig. 11. Simulation results of a stable100kVA DVR system

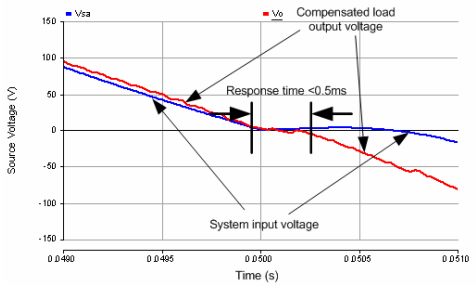

Fig. 12. DVR system response time

When phase A source-side system voltage meets 60% sag with 3rd, 5th and 7th harmonics at 0.05s, while the other phases remain unfaulted, provided that three-phase is under balanced nonlinear load, from Fig. 8, 10 and 11, the DVR can still compensate the load output voltage to the nominal value ($220V_{rms}$) with response time less than 0.5ms as in Fig. 12, which shows its capability of fast voltage sag and harmonics compensation. This simulation results also verify the per-unit system design for different DVR system capacity. From Fig. 9, the system parameters are designed based on the unstable per-unit values in Table III, it shows an unstable 10kVA system, with both load output voltage and DVR inject voltage increase to over 6000V. Simulation results of Fig. 8 – Fig. 11 also prove the previous analyses in system stability, voltage harmonics compensation capability, load adaptability and response time.

B. Experimental Results on a 10kVA DVR Prototype

In order to verify the simulation results, an experimental investigation of the DVR system was carried out in the laboratory. Fig. 1 depicts the system configuration of the DVR prototype and Fig. 13 illustrates a 10kVA DVR system performance in the laboratory tests (Note: Only the results of phase A are shown in the following).

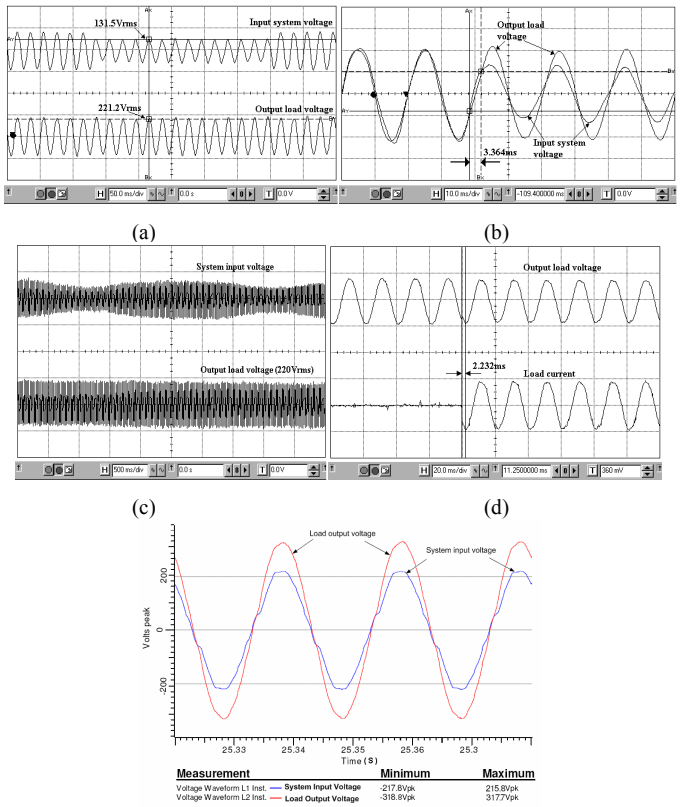

Fig. 13. Experimental results of a 10kVA DVR system. (a) Voltage sag compensation. (b) DVR response time. (c) Voltage flicker compensation. (d) Load sudden connected response time. (e) 30% voltage sag with harmonics compensation

DVR voltage compensation function is mainly focus on the system voltage sag, the system fault is assumed as single-phase voltage sag and voltage sag with harmonics and the three phases are having balanced resistive load of 30Ω (it can also

work in nonlinear load). When voltage sag happens in phase A, Fig. 13 (a) and (b) shows the experiment result of the voltage sag compensation. From Fig. 13 (a), even the system voltage meets 40.6% voltage sag, but the load output voltage still maintains to the nominal voltage level ($220V_{rms}$) regardless of the voltage disturbance happens. This experimental result will be the same for the other two phases if the same case happens. Fig. 13 (b) shows the DVR's response time on the voltage sag compensation, which is less than 5ms. When phase A system input voltage is varying rapidly, the load output voltage can still maintain its nominal level ($220V_{rms}$) regardless of the changes. Fig. 13 (c) shows the dynamic voltage flicker compensation capability of the DVR prototype. Fig. 13 (d) also clearly illustrates the DVR fast response (< 5ms) when load is suddenly connected. Finally, Fig. 13 (e) shows the experimental result of 30% voltage sag with harmonics compensation in phase A, which verifies the DVR harmonics and voltage sag compensation capability. The experimental results are consistent with the simulation results, and verify the per-unit system design approach and detailed analyses in system stability, voltage harmonics compensation capability, load adaptability and response time.

V. CONCLUSION

Based on the modeling of a transformerless, H-bridge double feedback loops DVR system, its stability, harmonics compensation capability, load adaptability and response time can both be investigated and analyzed. By using the per-unit system to design and analyze the system performances, those designed system parameters can also be applied to other capacity and base voltage systems conveniently, as it offers computational simplicity and also a more general manner than the physical unit system. The determination of DVR capacity and its corresponding DC storage capacitance and rating is also discussed. This research work can also act as a design reference for constructing different capacity transformerless, H-bridge double-loop control DVR from 1kVA to 100kVA. Finally, simulation and experimental results are presented to verify the per-unit design method and demonstrate a stable and good compensating feature.

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