System and Control Design of a Hybrid Active Power Filter in Three-Phase Four-Wire System

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Abstract–In this paper, the system implementation of a hybrid active power filter (HAPF) in three-phase four-wire power system is proposed and discussed. The HAPF is characterized by lower the dc-link rating of the conventional active power filter (APF) without significantly deteriorates the system compensation features and performances. An 110V/1.65KVA HAPF experimental prototype is built in a laboratory, and its experimental results are given in order to prove the correctness and effectiveness of the proposed HAPF.

Keywords–Power quality, hybrid active power filter.

I. INTRODUCTION

Due to the increase of non-linear load demands, a lot of harmonics (non-sinusoidal waveforms) occurred in power networks, which increases the transmission loss and may cause the system resonance between loads. Power system filters are the solution for the above described issues [1]–[3]. However, passive filter (PF) cannot be dynamically adjusted as a result they may cause system resonance between the filter and a load. On the other hand, the active power filter (APF) can be employed to compensate the harmonic components and reactive current dynamically. But, it required a high dc voltage inside the inverter so that the system rating and the cost are higher. A hybrid active power filter (HAPF) is a combination of a PF and an APF, which can reduce the system rating and initial cost but without significantly deteriorate the compensating and dynamic performances [2], [3].

In this paper, the system implementation of a HAPF under three-phase four-wire distribution power network is introduced and discussed. An 110V/1.65KVA HAPF experimental prototype is built successfully in a laboratory. The experimental compensation performances of the pure PF and the HAPF system with dc-link feedback controller will also be given and analyzed. The HAPF system is characterized by low dc-link rating with acceptable performances of compensating harmonic current, reactive power and neutral current. All the compensation results fulfilled the IEC 61 000-3-2 standard [4] and IEEE Power Quality 519:1992 standard [5].

II. HYBRID ACTIVE POWER FILTER (HAPF) IN THREE-PHASE FOUR-WIRE SYSTEM

Fig. 1 shows a three-phase four-wire HAPF circuit configuration. The determination of coupling capacitance C_c and inductance L_c were presented in [6], [7]. The generalized theory of instantaneous reactive power [8], [9] and Hysteresis PWM control are applied for APF reference current calculation and IGBT trigger signal determination.

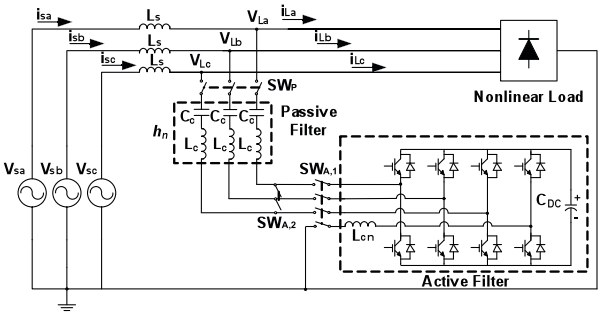


Fig. 1: A three-phase four-wire HAPF circuit configuration

III. AN 110V/1.65KVA EXPERIMENTAL HAPF IN THREE-PHASE FOUR-WIRE SYSTEM

A. Experimental system circuit configuration

Fig. 2 shows an 110V/1.65KVA HAPF experimental circuit configuration. The PF components C_c and L_c are designed according to the 5th resonance frequency order. On the other hand, the APF is composed of a dc-to-ac four-leg IGBT inverter with IGBT's drivers, transducers with signal conditioning boards, a DSP control board with AD sampling circuitry and an energy storage dc capacitor.

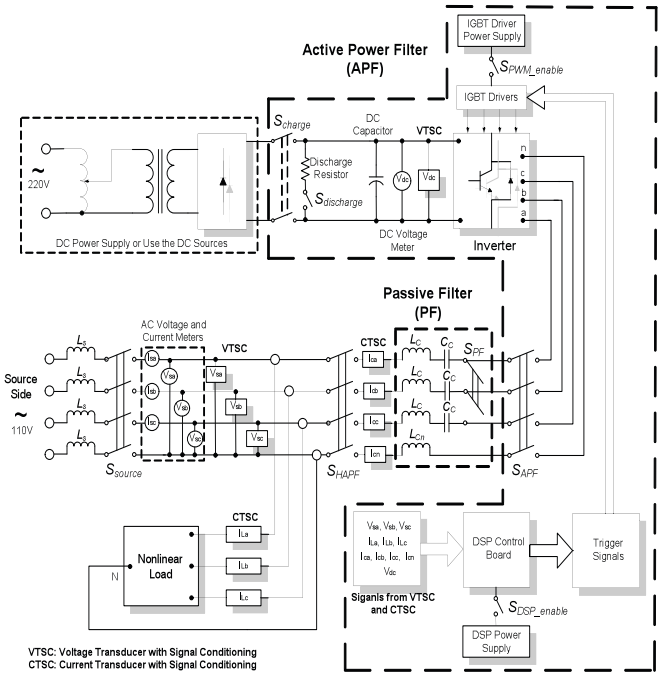
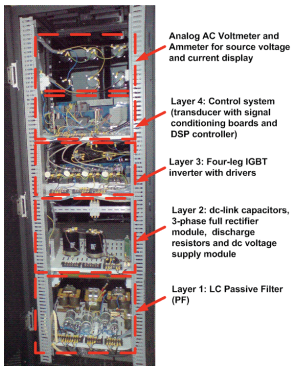


Fig. 2: An 110V/1.65KVA HAPF experimental circuit configuration

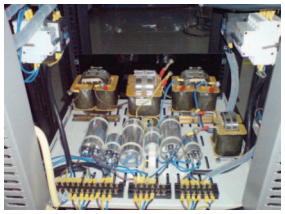
The DSP control board is based on a high speed Digital Signal Processor (D.S.P.) TMS320F2407. The transducers are based on the Hall effects, which can transform the electrical current and voltage into small signals. Additional signal conditioning circuits are designed to transfer the transducer output signals into a voltage range signal that can satisfy the requirements of the A/D conversion within the TMS320F2407 board. The DSP processes the sampled data, calculating the reference signal and generating trigger signals to the IGBT inverter with Hysteresis PWM control. The dc-link capacitor voltage is charging initially before compensation. The power supply of control system is given by an individual 220V source voltage with isolated transformer for protection.

Fig. 3 shows the photos of a three-phase four-wire capacitive-coupled HAPF experimental system.

(a) Front-view

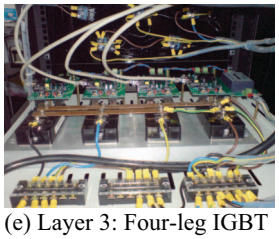


(b) Back-view

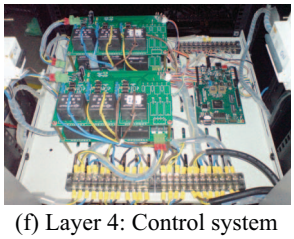


(c) Layer 1: LC Passive filter (PF)

(d) Layer 2: dc-link capacitors, 3-phase full rectifier module, discharge resistors and dc voltage supply module



(e) Layer 3: Four-leg IGBT inverter with drivers



(f) Layer 4: Control system (transducer with signal conditioning boards and DSP controller)

Fig. 3: Experimental system photos of the three-phase four-wire capacitive-coupled HAPF

B. Signal conditioning circuits

The voltage & current transducer with signal conditioning boards can transfer large electrical signals into small analog signals in order to be adopted as the inputs of DSP TMS320LF2407. The followings are the general introduction of the signal conditioning to adjust the sampling signal to satisfy the voltage requirements for the DSP. Fig. 4 shows a schematic diagram of the signal conditioning circuit. The resistance *R1* of current transducer KT 20 A/P is selected to be 50 Ω, while that of voltage transducer KV 50 A/P is selected to be 100 Ω. Thus, the maximum root mean square (rms) output voltage of the current and voltage transducers will be the same of $5V$, and the peak value is $5\sqrt{2}V$.

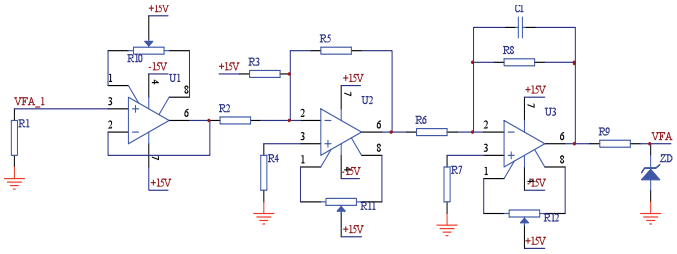


Fig. 4: A schematic diagram of the signal conditioning circuit

The maximum input voltage of TMS320LF2407 is 3.3V, hence, the peak output voltage of the signal conditioning part should be consistent with (0 ~ 3.3V) of the DSP. In order to avoid the unsteady state of DSP when the input voltage of DSP approaches 3.3V, the peak output voltage is changed to consistent with (0.35 ~ 2.95V) of the DSP. From Fig. 4, the signal conditioning equation can be deduced as:

$$v_o = \frac{R5}{R2} v_{in} + \frac{R5}{R3} \times 15 \text{ , } (v_{in} = VFA\_1, v_o = VFA) \qquad (1)$$

Select $R5 = 2.2k\Omega$, $R2 = 12k\Omega$, $R3 = 20k\Omega$, $R4 = 1.5k\Omega$, $R7 = 5k\Omega$ and $R6 = R8 = 10k\Omega$. $R10, R11, R12$ are $20k\Omega$ adjustable resistors for zero tuning. Take $v_{in\_max} = 5\sqrt{2}$ V and $v_{in\_min} = -5\sqrt{2}$ V, $v_{o\_max} = 2.95$ V and $v_{o\_min} = 0.35$ V. ZD is a zener diode of 3.3V. $R8$ and $C1$ form a first order low-pass filter, which aims at filtering the high frequency noise signal existed in the digital system.

C. DC-link power PI feedback controller design in DSP

From the active control block diagram model in [7], the proportional and integral gains (K_I , K_{II}) of the PI controller can be designed as:

$$\begin{cases} K_I = 0.565a \\ K_{II} = 0.00849a^2 \end{cases} \qquad (2)$$

Where a is the cut-off frequency of the lowpass filter. In order to realize the dc-link PI feedback controller with the DSP, the model of the feedback controller is required to be transformed from continuous-time model to discrete-time model. Since the response of the dc-link feedback control is limited by the controller cut-off frequency a, to provide a feedback control with small sampling error, the sampling frequency of the PI controller can be selected to be much larger than that of a. In this experimental system, the value of the controller cut-off frequency is selected as 25Hz, and the sampling frequency of the feedback controller is selected to be 500Hz. With the help of Z-transform function, the corresponding signal flow graph of the PI controller can be deduced and constructed for DSP programming flow, as shown in Fig. 5.

$$
\begin{aligned}
a_2 &= -\left(1+e^{-aT}\right) \\
a_3 &= e^{-aT} \\
b_1 &= \left(1-e^{-aT}\right)\left(K_I - \frac{K_{II}}{a}\right) + K_{II}T \\
b_2 &= -\left[\left(1-e^{-aT}\right)\left(K_I - \frac{K_{II}}{a}\right) + e^{-aT}K_{II}T\right]
\end{aligned} \tag{3}
$$

With the signal flow diagram, the corresponding dc-link feedback control subroutine can be programmed accordingly. The overall interrupt assignment and programming flowchart will be introduced in the following.

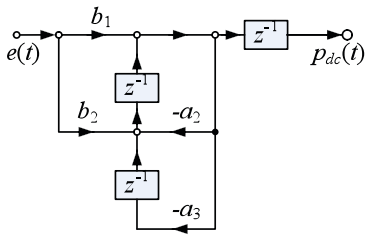


Fig. 5: Signal flow diagram of the dc-link PI feedback controller

D. DSP controller software design

The DSP controller TMS320LF2407 is required to implement the signal sampling and conditioning, instantaneous compensation algorithm, dc-link feedback control, and generating the PWM signal for controlling the output of the inverter. In this experimental system, the signal sampling, control algorithm calculation and PWM generation are implemented with DSP different timer interrupt subroutines.

1. A/D channels 2-13 are assigned to analog signals i_{Ca}, i_{Cb}, i_{Cc}; v_{dc}, *reserved*, i_{Cn}; i_{La}, i_{Lb}, i_{Lc} and V_{Sa}, V_{Sb}, V_{Sc}. In the DSP, the number and order of A/D channel selection can be programmed.
2. Timer 1 and Timer 3 are responsible for generating PWM. A/D conversion is loaded with Timer 4, and Timer 2 is left for signal processing. The frequency of Timer 1 and Timer 3 are determined by the requirement of PWM, the period of Timer 4 is set to be 20 kHz (which is the sampling frequency), and the period of Timer 2 is 5kHz. In hysteresis PWM, the PWM switching table in decided in Timer 4, and it defines the PWM frequency.
3. Interrupts: Only two interrupts are activated. The A/D interrupt is at highest priority, and the second is Timer 2 interrupt.

The flowchart of the DSP main routine and the timer subroutines are shown in Fig. 6. Since A/D interrupt is responsible for fast PWM reference signal decisions, the determination of the reference current is executed in Timer 2 subroutine. In this arrangement, a trade-off could be made between data sampling frequency and routine implementation time with different timer for PWM processing and data processing. Since the frequency of the reference source current is only 50Hz, Timer 2 with lower sampling frequency can handle the reference source current processing with adequate precision. It is beneficial for the design of lowpass filter required for the instantaneous reactive power compensation algorithm, and the application of PI controller in the feedback control of the dc-link voltage, which requires long routine processing.

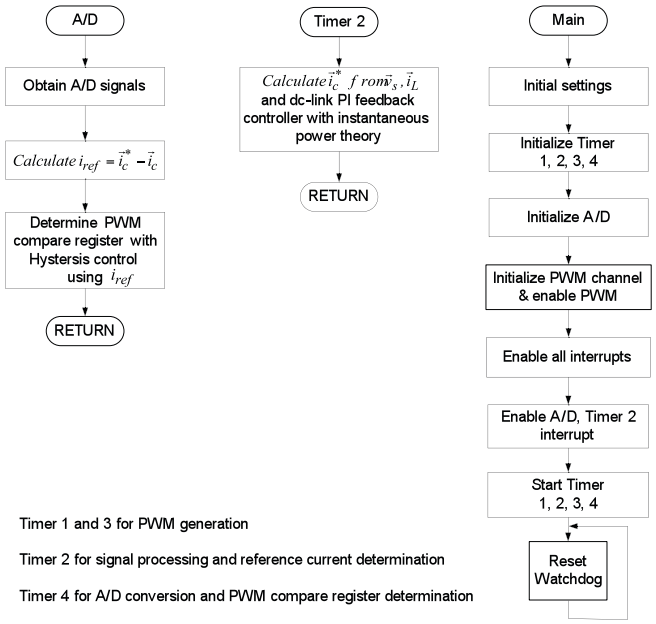


Fig. 6: Flowchart of the HAPF DSP program

IV. Experimental Results

The technical data of an 110V/1.65kVA HAPF experimental system is given in Table 1. The dead-time of the IGBT is set to $5.3\mu s$, which can guarantee the safety of IGBT operation without deteriorate the system performance.

Table 1: Technical data of an 110V/1.65kVA capacitive-coupled HAPF experimental system

System Parameters	Value
Capacity	1.65 kVA
Source, load voltage magnitude	110V/50Hz
Source inductance L_s	1.3mH
Filtering inductance L_c, L_{cn}	5.0mH, 2.0mH
Filtering capacitance C_c	81.0μF
dc storage capacitance C_{dc}	20mF
dc-link reference voltage V_{dc0}	15V
Filter frequency a	$a = 2\pi 25$
PI proportional and integral gains K_I, K_{II}	$\begin{cases} K_I = 0.565a \\ K_{II} = 0.00849a^2 \end{cases}$ [7]
PWM control	Hysteresis PWM (comparator period = 14.6kHz)

To prove the validity and effectiveness of the displacement power factor, power factor, harmonics and imbalance current compensation with the HAPF, the experimental system is equipped with a set of nonlinear load. In the experiment, three single-phase full rectifiers are adopted to imitate the nonlinear load of computer power supply commonly existed. The main harmonics are

in triple and fifth harmonic orders. The nonlinear load is balanced with load current = 4.8Arms and load power factor =0.85. The experimental waveforms before and after PF and HAPF compensation will be shown in the following.

A. Before compensation

The experimental waveforms of the load voltages, source currents, load currents, neutral current and power factor waveforms captured with scope DL750 are shown in Figs. 7a and 7b, in which the three-phase displacement power factor and power factor are 0.85, 0.82. In addition, the source current THD taken by Fluke are 22%. Since the IEC 61 000-3-2 standard acceptable THD for load smaller than 16A per phase is at 16% [4], thus the source current THD falls outside the standard acceptable range before compensation. Moreover, the load voltage THD of 5.2% falls outside the IEEE standard 519:1992 acceptable range (THDv <5%) [5]. The neutral current before compensation is 2.96Arms.

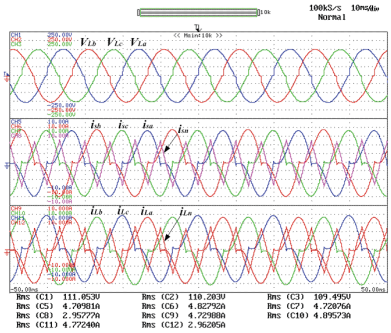


Fig. 7a: Three-phase load voltage, source current, load current and neutral current before compensation

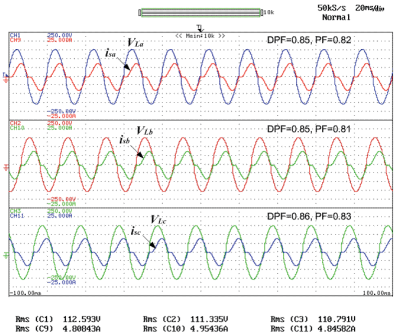


Fig. 7b: Three-phase power factor before compensation

B. After pure passive filter (PF) compensation

The load voltage, source current, load current and neutral current waveforms after PF compensation are shown in Fig. 8a. From Fig. 8b, the source current has been compensated to be almost in-phase with load voltage. Since the PF is fine tuned to the 5th harmonic order, the 5th harmonic components have been greatly reduced. However, the source current THD is increased from original 22% to 24.5% after the PF compensation, which falls outside the IEC 61 000-3-2 standard 16%. This is due to the decrease of the source current fundamental component. Since the PF supplies the required fundamental reactive current to the loading, the original source current fundamental reactive components will be decreased, thus causing a deterioration of the THD phenomenon. Compared with Fig 7b, the displacement power factor and power factor have been significantly improved to over 0.99 and 0.95 as shown in Fig 8b. Moreover, the load voltage THD of 4.7% falls within the IEEE standard 519:1992 (THDv <5%) after PF compensation.

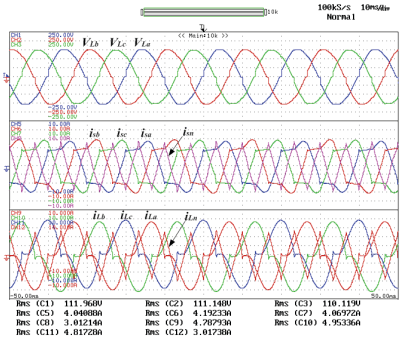


Fig. 8a: Three-phase load voltage, source current, load current and neutral current after PF compensation

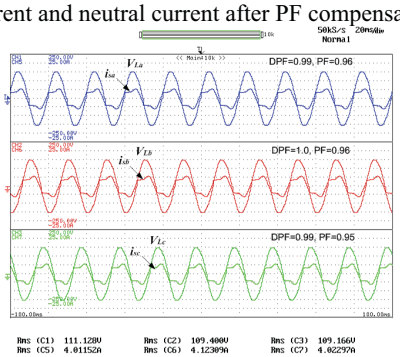


Fig. 8b: Three-phase power factor after PF compensation

C. After hybrid active filter (HAPF) compensation

The load voltage, source current, load current, neutral current, dc-link voltage and APF injecting current waveforms after HAPF compensation can be shown in Fig. 9. Fig. 9a shows the three-phase load voltage, source current, load current, neutral current and dc-link voltage waveforms after HAPF compensation. From Fig. 9b, the source current has been compensated to be sinusoidal and in-phase with load voltage, while the source current THD been improved from 22% to 7%, which falls within the IEC 61 000-3-2 standard 16%. Compared with Fig 7b, the displacement power factor and power factor have significantly improved to 1.0 and 0.99 from the original around 0.85, 0.82 as shown in Fig 9b. Moreover, the load voltage THD of 2.7% falls within the IEEE standard 519:1992 (THDv <5%). The neutral current has also been compensated from 2.96 Arms to 0.88 Arms. Fig. 9c shows the APF operating current of 2.97Arms and dc-link voltage of 15V at steady-state.

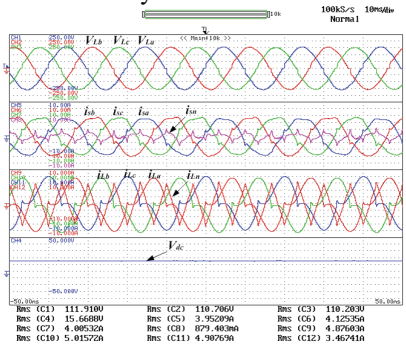


Fig. 9a: Three-phase load voltage, source current, load

current and neutral current after HAPF compensation

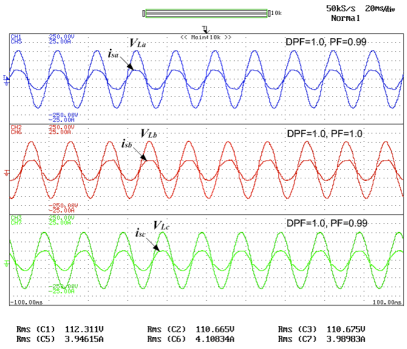


Fig. 9b: Three-phase power factor after HAPF compensation

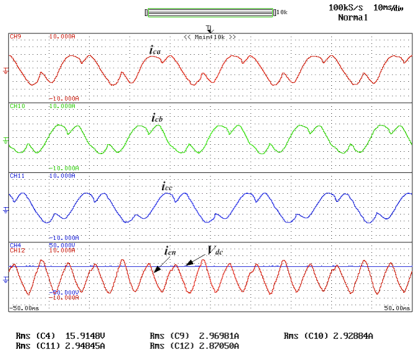


Fig. 9c: HAPF inject current and dc-link voltage

Compared the results with pure PF case, the HAPF can further improve the compensating performance with low dc-link voltage supply of 15V at this load situation (having 95% reduction of the pure APF minimum voltage level requirement). Moreover, compensation of the current harmonics benefits to the voltage quality problem. Table 2 summarizes the three-phase compensation performances before and after PF and HAPF operation.

Table 2: Summarizes three-phase compensation performances before and after PF and the HAPF operation

	THD of Source Current i_{sa} (%)			Source Neutral Current i_{sn} (A_{rms})	Displacement Power Factor (DPF) and Power Factor (PF)		
	A	B	C	N	A	B	C
No Filter	21.8	21.6	22.4	2.96	0.85, 0.82	0.85, 0.81	0.86, 0.83
PF	23.6	24.4	25.7	3.01	0.99, 0.96	1.0, 0.96	0.99, 0.95
HAPF	6.9	7.0	7.2	0.88	1.0, 0.99	1.0, 1.0	1.0, 0.99

(a)

	THD of Load Voltage V_{La} (%)			Inverter Operating Current (A_{rms})			
	A	B	C	A	B	C	N
No Filter	4.8	5.2	5.2	---	---	---	---
PF	4.3	4.7	4.6	---	---	---	---
HAPF	2.7	2.9	2.7	2.97	2.93	2.95	2.87

(b)

V. Conclusion

In this paper, the system implementation of an 110V/1.65KVA three-phase four-wire HAPF experimental prototype with dc-link feedback controller are discussed and analysed. Experimental results are given to verify the correctness and effectiveness of the HAPF system in power quality compensation. The HAPF is characterized with low dc-link rating and good performances in current harmonics, neutral current, displacement power factor and power factor compensation. The compensation effect is also benefit for the voltage quality problem.

Acknowledgment

The authors would like to thank the Science and Technology Development Fund, Macao SAR Government and University of Macau for their financial supports.

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