Three-dimensional space vector modulation with DC voltage variation control in a three-leg centre-split power quality compensator

N.Y. Dai, M.C. Wong and Y.D. Han

Abstract: Three-dimensional space vector modulation (3DSVM) is proposed for controlling a three-leg centre-split inverter, which is used as a shunt power quality compensator for a three-phase four-wire system. Important issues for 3DSVM, such as 3D space vector allocation, zero-sequence compensation and DC voltage variation, are discussed in detail. In the two-level three-leg centre-split system, all eight vectors contribute to the zero-sequence compensation, which is different from the conventional two-dimensional compensation. Hence, the 3DSVM control strategy is more complicated than conventional 2DSVM. Particularly, in a two-level system there is no null vector in 3D case such that the zero state is approximated by two zero vectors, which directly point in positive and negative zero-axis, respectively. Results indicate that the original reference of the 3D vector's allocation is affected by DC voltage variation only along the zero-frame. Conversely, the DC voltage variation can be controlled by adjusting the origin of 3D reference. Simulation results are given to show the validity of the proposed control strategy: 3DSVM with DC voltage variation control. A two-level three-leg centre-split inverter prototype is implemented and controlled by a digital signal processor with 2.5 kHz switching frequency. Experimental results are also presented to show its validity.

1 Introduction

Due to the development of the 'custom power' concept, the three-phase four-wire system will play a very important role in the distribution site. Past research indicates that there are, primarily, two ways [1] to provide neutral current compensation in a three-phase four-wire system via three-phase voltage-source inverters: using split DC capacitors and tying the neutral wire to the mid-point of the DC-linked capacitors: using a four-leg converter topology and tying the neutral wire to the mid-point of the fourth neutral leg. Compared with the four-leg converter, the three-leg centre-split converter uses fewer switching devices, thereby reducing the initial cost. The main drawbacks of three-leg centre-split inverters are that their control strategy is relatively complicated as compared to the four-leg one, and that the DC voltage utility ratio is relatively lower in a two-level structure.

Corresponding to the adoption of the inverter structure, PWM control techniques must be extended from two into three-dimensions. The mid-point of the DC linked capacitors of the three-leg centre-split inverter is connected with the neutral wire in the three-phase four-wire system. The three-phase centre-split inverter becomes three independent single-phase half-bridge inverters. Thus, compensating currents flow through the upper or lower capacitor due to different switching states. As a result, DC voltage variation occurs and this influences the compensation performance. The issues of DC voltage variation should be considered and controlled in practical applications. In 2002, a three-dimensional space vector PWM (3DSVM) for a four-leg converter was proposed [2]. In past research into PWM control only *a-b-c* [1] and α-β-0 hysteresis control [5, 6] strategies have been presented for controlling the three-leg centre-split inverter system. Thus far there has been no report of the 3DSVM and DC voltage variation control under $\alpha\beta0$ frame consideration for the three-leg centre-split inverter. In this paper, the 3DSVM with DC voltage variation control for the three-leg centre-split inverter is discussed in detail. This can compensate the harmonic, reactive currents as well as the neutral current in three-phase four-wire system simultaneously. Simulation and experimental results are given to show the validity of power quality compensation together with DC voltage variation control.

2 Basic principle of 3DSVM

In this paper, the three-leg 'centre-split' inverter structure [1] is the basic configuration for the discussion of three-dimensional pulse-width modulation. Figure 1 shows a two-level centre-split inverter which is used as a shunt power quality compensator for a three-phase four-wire system.

2.1 Three-dimentional voltage vector allocation

It is assumed that the upper-arm and the lower-arm capacitor voltages in Fig. 1 are the same, i.e. Vdc1 =

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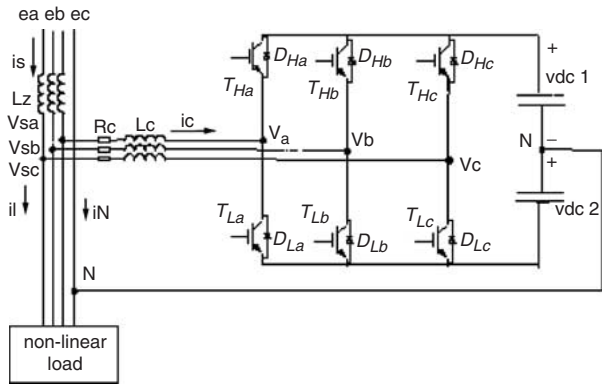

Fig. 1 *'Centre-split' inverter as a power quality compensator*

Vdc2 = Vdc. The switching function can be defined as:

$$S_j = \begin{cases} 1 & \textit{upper leg is on} \\ -1 & \textit{lower leg is on} \end{cases} \quad j = a, b, c \tag{1}$$

Thus, the output voltage of one leg of the inverter can be expressed as:

$$v_j = V_{dc} * S_j \quad j = a, b, \mathrm{c} \tag{2}$$

The instantaneous voltage vector in *a-b-c* frame can be described as shown in (3):

$$\vec{v} = \sqrt{\frac{2}{3}}(v_a + \alpha \cdot v_b + \alpha^2 \cdot v_c) \tag{3}$$

where $\alpha = e^{j\frac{2\pi}{3}}, \alpha^2 = e^{-j\frac{2\pi}{3}}$.

According to (4), the instantaneous voltage can be transferred from *a-b-c* frame to α-β-0 frame:

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/\sqrt{2} & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{4}$$

Based on the switching function definition and the α-β-0 frame transformation, the instantaneous voltage vector in α-β-0 frame can be given as:

$$\overrightarrow{v} = V_{dc}\left[\sqrt{\frac{2}{3}}S_\alpha \cdot \vec{n}_\alpha + \frac{1}{\sqrt{2}}S_\beta \cdot \vec{n}_\beta + \frac{1}{\sqrt{3}}S_0 \cdot \vec{n}_0\right] \tag{5}$$

where $S_\alpha = S_a - \frac{1}{2}S_b - \frac{1}{2}S_c$

$S_\beta = S_b - S_c$

$S_0 = S_a + S_b + S_c$.

It can also be expressed in α-β-0 frame as:

$$\vec{v} = v_\alpha \vec{n}_\alpha + v_\beta \vec{n}_\beta + v_0 \vec{n}_0 \tag{6}$$

where $v_\alpha = V_{dc} \cdot \sqrt{\frac{2}{3}}S_\alpha, v_\beta = V_{dc} \cdot \frac{1}{\sqrt{2}}S_\beta, v_0 = V_{dc} \cdot \frac{1}{\sqrt{3}}S_0$.

The 3DPWM voltage vectors can be described in *a-b-c* and in α-β-0 frame respectively, as shown in Table 1. Figure 2 shows the two-level voltage vector's allocation in 3D aspect. The vectors $\{\vec{V}_2, \vec{V}_4, \vec{V}_6\}$ and $\{\vec{V}_1, \vec{V}_3, \vec{V}_5\}$ lie on the different horizontal levels and the zero vectors $\{\vec{V}_{0p}, \vec{V}_{0n}\}$ are the directional vectors pointing in the positive and negative zero-axes, respectively. The conventional space vector's allocation of two-level inverter in α-β frame is shown in Fig. 3. It is obvious that the projection of actual space vector allocation in 3D frame on the α-β plane is identical with the conventional two-dimentional space vector allocation.

Table 1: Two-level 3DPWM voltage vector

	S_a	S_b	S_c	S_α	S_β	S_0
$\vec{V}_1$	1	−1	−1	2	0	−1
$\vec{V}_2$	1	1	−1	1	2	1
$\vec{V}_3$	−1	1	−1	−1	2	−1
$\vec{V}_4$	−1	1	1	−2	0	1
$\vec{V}_5$	−1	−1	1	−1	−2	−1
$\vec{V}_6$	1	−1	1	1	−2	1
$\vec{V}_{00p}$	1	1	1	0	0	3
$\vec{V}_{00n}$	−1	−1	−1	0	0	−3

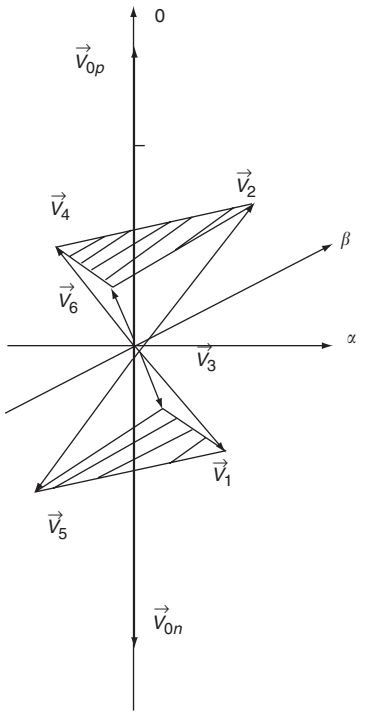

Fig. 2 *Two-level 3D voltage vector's allocation*

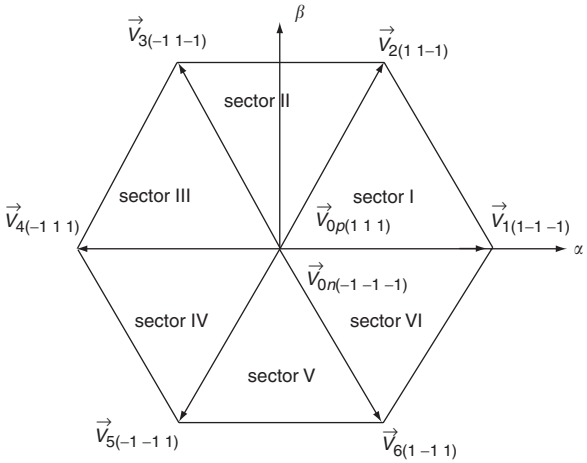

Fig. 3 *Voltage space vector's allocation in α-β frame*

2.2 Control strategy of 3DSVM

In three-dimentional space vector modulation (3DSVM) technique, the voltage-second reference can be approximated by a sequence of voltage-second states as shown in (7) and (8). The vectors, $\vec{V}_x, \vec{V}_y$ and $\vec{V}_0$, are chosen, as they

are neighbouring vectors of the reference vector on α-β plane. The neighbouring vectors on the apex of the hexagon, as shown in Fig. 3, are such that when the output of the inverter changes from one vector to another neighbouring one, only the switching state of one leg needs to be changed accordingly. Based on this property, the optimum switching sequence scheme can be implemented and the output harmonics of the inverter can be reduced [2]. However, the vectors $\vec{V}_x$ and $\vec{V}_y$ contribute to the zero-sequence component as well as the α-β plane compensation to the reference vector, which is different from conventional 2DSVM. The vector $\vec{V}_0$ contributes to zero-sequence compensation only and can be chosen according to the required zero-axis or neutral current compensating component. The product of $\vec{V}_{zero}t_{zero}$ should be equal to zero in the sense that t_{zero} is the redundant time in one compensation period. In the case of over-modulation, t_{zero} is equal to zero.

$$\vec{V}^*_{ref}T_S = \vec{V}_x t_x + \vec{V}_y t_y + \vec{V}_0 t_0 + \vec{V}_{zero}t_{zero} \tag{7}$$

$$t_{zero} = T_S - t_x - t_y - t_0 \tag{8}$$

Actually, the reference vector $\vec{V}^*_{ref}$ can be described in three-dimensional aspect as:

$$\vec{V}^*_{ref} = \vec{V}^*_\alpha \vec{n}_\alpha + \vec{V}^*_\beta \vec{n}_\beta + \vec{V}^*_0 \vec{n}_0 \tag{9}$$

The formula for calculating the switching time t_x, t_y, t_0 can be expressed in a general form (10). The matrix [Ag] can be expressed in six forms according to the sector location of reference vector $\vec{V}^*_{ref}$. After the sector location of $\vec{V}^*_{ref}$ is detected in Fig. 3, the corresponding section location value 'g' can be determined:

$$[V^*_{ref}] = m[A_g][t_{xy0}] \tag{10}$$

$$g = \mathrm{I}, \mathrm{II}, \mathrm{III}, \mathrm{IV}, \mathrm{V} \text{ or } \mathrm{VI}.$$

$$A_I = \begin{bmatrix} 1 & \cos 60^0 & 0 \\ 0 & \sin 60^0 & 0 \\ -C\cos k & C\cos k & C \end{bmatrix}$$

$$A_{II} = \begin{bmatrix} \cos 60^0 & -\cos 60^0 & 0 \\ \cos 30^0 & \cos 30^0 & 0 \\ C\cos k & -C\cos k & C \end{bmatrix}$$

$$A_{III} = \begin{bmatrix} -\cos 60^0 & -1 & 0 \\ \cos 30^0 & 0 & 0 \\ -C\cos k & C\cos k & C \end{bmatrix}$$

$$A_{IV} = \begin{bmatrix} -1 & -\cos 60^0 & 0 \\ 0 & -\cos 30^0 & 0 \\ C\cos k & -C\cos k & C \end{bmatrix}$$

$$A_V = \begin{bmatrix} -\cos 60^0 & \cos 60^0 & 0 \\ -\cos 30^0 & -\cos 30^0 & 0 \\ -C\cos k & C\cos k & C \end{bmatrix}$$

$$A_{VI} = \begin{bmatrix} \cos 60^0 & 1 & 0 \\ -\cos 30^0 & 0 & 0 \\ C\cos k & -C\cos k & C \end{bmatrix}$$

where

$$m = \frac{2 \cdot \sqrt{\frac{2}{3}} \cdot V_{dc}}{T_S} C = \frac{3}{2 \cdot \sqrt{2}} \text{ and } k = 70.54^0$$

In conventional two-dimentional pulse-width modulation techniques, among the eight available voltage vectors there are six directional vectors and two zero vectors, $\vec{V}_{0p}$ and $\vec{V}_{0n}$. As no injecting action is performed by choosing $\vec{V}_{0p}$ or $\vec{V}_{0n}$, either of these two zero vectors can be substituted for the net zero vector, $\vec{V}_{zero} = 0$. Both of the two vectors can be chosen according to the requirements of the sequence scheme. However, in a 3D two-level centre-split inverter system there are eight directional vectors corresponding to eight available vectors. When Fig. 2 is referred to, these vectors, $\vec{V}_{0p}$ and $\vec{V}_{0n}$, are not zero. In 3DPWM, these two vectors are dedicated as the zero-axis voltage component in positive or negative direction, and they are used to compensate neutral current in the three-phase four-wire system. The issue of $\vec{V}_{zero}t_{zero}$ can be solved by the exercise of the same amount of switching times, $t_{0p} = t_{0n}$, so that the approximated procedure for $\vec{V}_{zero}t_{zero} = 0$ can be obtained as:

$$\vec{V}_{0p}t_{0p} + \vec{V}_{0n}t_{0n} \approx \vec{V}_{zero}t_{zero} \approx 0 \tag{11}$$

Furthermore, according to the compensation requirement, $\vec{V}_{0n}$ is activated for negative zero-current injection into the neutral wire and $\vec{V}_{0p}$ is activated for positive zero-current injection, so that $t_{0p} \neq t_{0n}$ may occur for the neutral current compensation. In general, (7) should be replaced by (12).

$$\vec{V}^*_{ref}T_S = \vec{V}_x t_x + \vec{V}_y t_y + \vec{V}_{0n}t_{0n} + \vec{V}_{op}t_{op} \tag{12}$$

The switching times are calculated under two conditions: under-modulation and over-modulation.

Case 1: Under-modulation

After t_x, t_y and t_0 are obtained from (10), t_{0p} and t_{0n} in (12) can be decided accordingly. The consideration of $\vec{V}_{zero}$ t_{zero} is taken as actual null, i.e. there must be null output in all axes.

Positive zero vector is required:

$$\begin{cases} t_{0p} = t_0 + \dfrac{t_{zero}}{2} \\ t_{0n} = \dfrac{t_{zero}}{2} \end{cases} \tag{13}$$

Negative zero vector is required:

$$\begin{cases} t_{0p} = \dfrac{t_{zero}}{2} \\ t_{0n} = t_0 + \dfrac{t_{zero}}{2} \end{cases} \tag{14}$$

Case 2: Over-modulation

In the case of over-modulation, the switching times t'_x, t'_y and t'_0 are simply computed from the original voltage vector and then modified according to the geometrical relationship, and assuming $t_{zero} = 0$.

$$t'_x = \frac{t_x}{t_x + t_y + t_0} T_s \tag{15}$$

$$t'_y = \frac{t_y}{t_x + t_y + t_0} T_s \tag{16}$$

Positive zero vector is required:

$$\begin{cases} t'_0 = t_{0p} = \dfrac{t_0}{t_x + t_y + t_0} T_s \\ t_{0n} = t_{zero} = 0 \end{cases} \tag{17}$$

Negative zero vector is required:

$$\begin{cases} t_0' = t_{0n} = \dfrac{t_0}{t_x + t_y + t_0} T_s \\ t_{0n} = t_{zero} = 0 \end{cases} \tag{18}$$

The control scheme of 3DSVM for a shunt power quality compensator is shown in Fig. 4. The determination of the instantaneous reference current for compensation is discussed in generalized instantaneous reactive power theory [7] for a three-phase four-wire system: this paper is not focused on reference current determination.

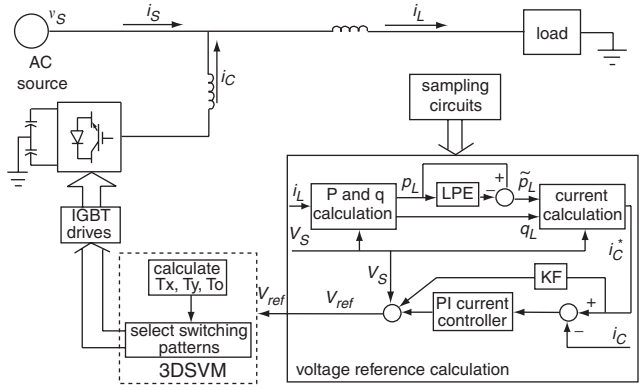

Fig. 4 *Control scheme of 3DSVM*

3 DC voltage control

3.1 Analysis of DC voltage variation

In the three-leg centre-split inverter structure as shown in Fig. 1, the AC neutral wire is connected directly to the mid-point of the two DC-linked capacitors. When the neutral current is compensated, current will flow in or out of the mid-point of the DC-linked capacitors. As the currents passing through the capacitors C_1 and C_2 are different, DC voltage variation occurs. The relationship between the phase current and the DC voltage variation is explained in detail in [1].

After the DC voltage variation is considered, the switching function defined in (1) must be modified accordingly. In the following analysis, S_j is defined as the switching function where the effect of DC voltage variation is not considered, and S_j^N is the new switching function where the DC voltage variation is considered. When $V_{dc1} \neq V_{dc2}$ is employed, V_{dc} can be redefined as $V_{dc} = (V_{dc1} + V_{dc2})/2$. Thus, the corresponding new switching function is described as:

$$S_j^N = \begin{cases} V_{dc1}/V_{dc} \; upper - leg \; is \; on \\ -V_{dc2}/V_{dc} \; lower - leg \; is \; on \end{cases} \; j = a, b, c \tag{19}$$

And $S_j^N =$

$$\begin{cases} \dfrac{V_{dc1}}{V_{dc}} = \dfrac{2 * V_{dc1}}{V_{dc1} + V_{dc2}} = \dfrac{V_{dc1} + V_{dc2} + V_{dc1} - V_{dc2}}{V_{dc1} + V_{dc2}} \\ \quad = 1 + \dfrac{V_{dc1} - V_{dc2}}{V_{dc1} + V_{dc2}} \\ -\dfrac{V_{dc2}}{V_{dc}} = \dfrac{2 * V_{dc2}}{V_{dc1} + V_{dc2}} = \dfrac{-(V_{dc1} + V_{dc2}) + V_{dc1} - V_{dc2}}{V_{dc1} + V_{dc2}} \\ \quad = -1 + \dfrac{V_{dc1} - V_{dc2}}{V_{dc1} + V_{dc2}} \end{cases} \tag{20}$$

If $\Delta S = (V_{dc1} - V_{dc2})/(2 * V_{dc})$ is substituted into (20), it can be simplified as:

$$S_j^N = \begin{cases} 1 + \Delta S \\ -1 + \Delta S \end{cases} \quad j = a, b, c \tag{21}$$

Comparing (21) with (1), the relation between the new switching function and the original one can be expressed as:

$$S_j^N = S_j + \Delta S \tag{22}$$

Hence, the output voltage of the inverter can be recalculated by these new S_a^N, S_b^N and S_c^N. The instantaneous voltage vector $\vec{v}^N$ in 3D, α-β-0 coordinate, can be expressed as:

$$\vec{v}^N = V_{dc}\left[\sqrt{\frac{2}{3}} S_\alpha^N \cdot \vec{n}_\alpha + \frac{1}{\sqrt{2}} S_\beta^N \cdot \vec{n}_\beta + \frac{1}{\sqrt{3}} S_0^N \cdot \vec{n}_0\right] \tag{23}$$

$$\text{where:} \quad S_\alpha^N = S_a^N - \frac{1}{2} S_b^N - \frac{1}{2} S_c^N \tag{24}$$

$$S_\beta^N = S_b^N - S_c^N \tag{25}$$

$$S_0^N = S_a^N + S_b^N + S_c^N \tag{26}$$

Substituting the new switching function (22) into (24), (25) and (26):

$$S_\alpha^N = S_\alpha \tag{27}$$

$$S_\beta^N = S_\beta \tag{28}$$

$$S_0^N = S_0 + 3\Delta S \tag{29}$$

As a result, only the zero-frame reference of the original 3D vector's allocation is changed under the DC voltage variation situation, and only the compensation performance of the zero-frame is affected accordingly. However, when the output voltage is reversely transformed to a-b-c frame, current compensation in each phase will be affected. Thus, the issues of DC voltage variation must be controlled in practical applications, and as such the DC voltage variation control strategy is proposed.

3.2 DC voltage variation control strategy for 3DSVM

In the space vector's allocation which is shown in Fig. 2, there are two switching patterns for the zero voltage vectors: one positive ($\vec{V}_{0p}$) and ore negative ($\vec{V}_{0n}$). The α and the β axes components of $\vec{V}_{0p}$ and $\vec{V}_{0n}$ are equal to zero. According to the results obtained in the preceding Section, the DC voltage variation affects only the zero-frame reference. Hence, DC voltage variation is controlled by varying switching times of $\vec{V}_{0p}$ and $\vec{V}_{0n}$.

Figure 5 shows the current direction when the vector $\vec{V}_{0p}$ or $\vec{V}_{0n}$ is chosen. It is obvious that the inverter's current only passes through one of the DC capacitors when the voltage vector is $\vec{V}_{0p}$ or $\vec{V}_{0n}$. When the output vector of the inverter

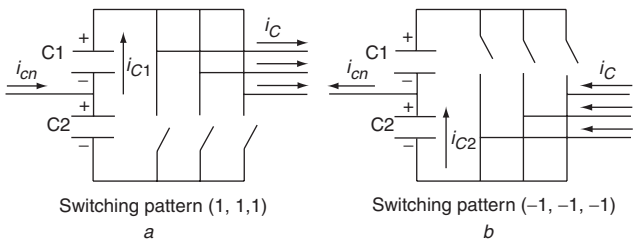

Fig. 5 *Phase current under zero switching pattern*

Table 2: Relation of DC voltage and ε

Cases	Condition	ε
Serious dc Voltage Imbalance	$abs(deltav) > V_{max}$	*
Largest Lower Voltage Imbalance	$-V_{max} < deltav < -k \cdot V_{dc}$	−1
Larger Lower Voltage Imbalance	$-k \cdot V_{dc} < deltav < 0$	$deltav/(k \cdot V_{dc})$
Larger Upper Voltage Imbalance	$0 < deltav < k \cdot V_{dc}$	$deltav/(k \cdot V_{dc})$
Largest Upper Voltage Imbalance	$k \cdot V_{dc} < deltav < V_{max}$	+1

is $\vec{V}_{0p}$, which corresponds to the switching pattern (1, 1, 1), the upper capacitor C_1 is discharged. Reversely, if the output vector is $\vec{V}_{0n}$, corresponding to the switching pattern (−1, −1, −1), the lower capacitor C_2 is discharged. Therefore $\vec{V}_{0p}$ and $\vec{V}_{0n}$ can change the DC voltage imbalance in opposite directions.

In the 3DSVM control technique, $\vec{V}^*_{0p}$ and $\vec{V}^*_{0n}$ share the same dwell-time $t_{zero}/2$ to approximate to $V_{zero}t_{zero} = 0$. Hence, if the dwell-times of $\vec{V}^*_{0p}$ and $\vec{V}^*_{0n}$ are varied, the output of $V_{zero}t_{zero}$ will not be equal to zero. However, since the α and the β axis components of $\vec{V}^*_{0p}$ and $\vec{V}^*_{0n}$ are all zero, the $V_{zero}t_{zero}$ only have a zero-sequence output. In the proposed DC variation control strategy, a new variable, $\varepsilon(0 < \varepsilon < 1)$, is introduced to vary the dwell-times of $\vec{V}^*_{0p}$ and $\vec{V}^*_{0n}$, i.e. the dwell-time of $\vec{V}^*_{0p}$ is assigned to be $(1+\varepsilon)t_{zero}/2$, and thereby the dwell-time of $\vec{V}^*_{0n}$ automatically takes $(1-\varepsilon)t_{zero}/2$. Different ε value corresponds to different $V_{zero}t_{zero}$ output, which is employed to balance the neutral point voltage. This method is often used for balancing the DC voltage of the tri-level neutral-point-clamped inverter [8].

Further, the larger the value of ε, the higher the DC control ability. Thus, it is reasonable to consider choosing ε as one or minus one to maximize the ability of the DC voltage variation control in the time range of t_{zero}. The relation of DC voltage variation and ε values are listed in Table 2, where k is the proportional coefficient with $0 < k < 1$ and V_{dc} is the reference DC voltage. The '*deltav*' can be calculated by the expression described in (30). However, there is a symbol '*' which means 'cannot be defined' in Table 3 when the '*deltav*' exceeds the maximum DC variation limitation, V_{max}. If the detected DC voltage imbalance is too large, it will affect the stability of the system. In that case, the control strategy in Table 3 can be considered, in which the whole period of sampling time T_s is employed to control the DC voltage variation.

Table 3: Time distribution under severe DC imbalance case

Condition	Dwell time of $\vec{V}^*_{0p}$	Dwell time of $\vec{V}^*_{0n}$
$deltav > V_{max}$	T_S	0
$deltav < -V_{max}$	0	T_S

$$deltav = abs(v_{dc1}) - abs(v_{dc2}) \tag{30}$$

4 Simulation results

Here, simulation is performed by Matlab/Simulink. The system configuration is shown in Fig. 1. The 3DSVM control strategy is implemented with 2.5 KHz switching frequency. The three-phase and the neutral current at the load side are shown in Fig. 6. When the proposed 3DSVM (without controlling the DC voltage variation) is applied, the harmonic and neutral currents are compensated simultaneously as shown in Fig. 7. Particular loads are chosen in this simulation, for which the system neutral current is always positive without compensation. Thus, there is a greater possibility of neutral current passing through one side of the inverter's DC bus, e.g. upper capacitor. As a result, the voltage on one capacitor continues to increase while the voltage on the other one

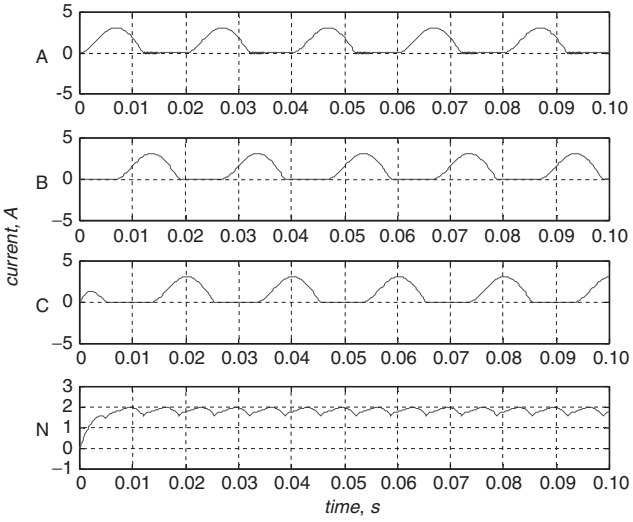

Fig. 6 *Load current*

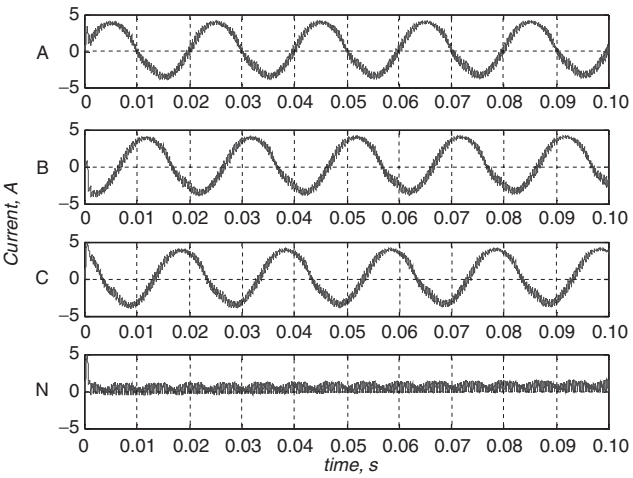

Fig. 7 *Source current after compensation by using 2.5 KHz 3D SVPWM*

continues to decrease. A large DC voltage unbalance occurs under this situation, which is shown in Fig. 8.

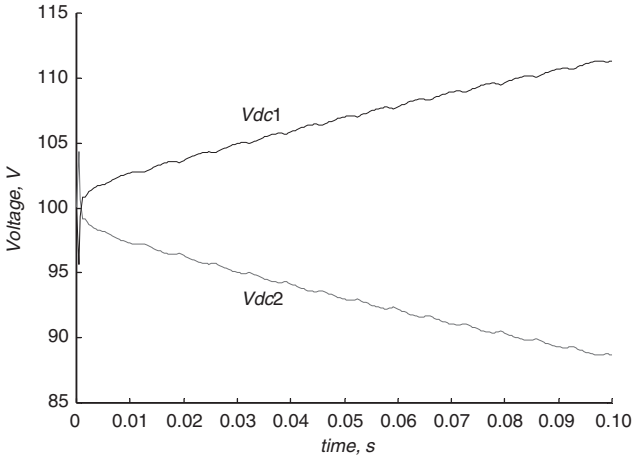

Fig. 8 *DC voltage without being controlled*

Figures 9 and 10 show the compensation results when the 3DSVM with DC voltage variation control is implemented.

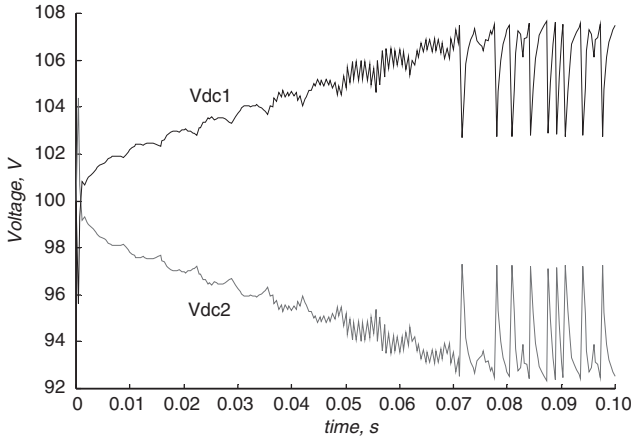

Fig. 9 *DC Voltage after being controlled*

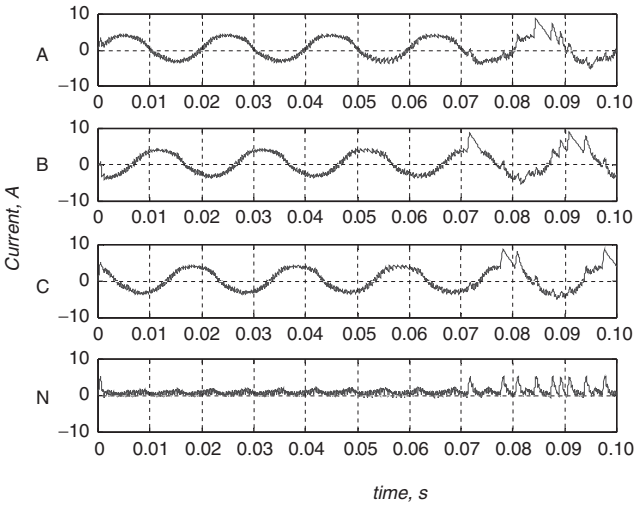

Fig. 10 *Source current after DC voltage variation control is added*

The control strategy mentioned in Tables 2 and 3 are employed to control the DC voltage variation. The capacitor voltage variation after being controlled is shown in Fig. 9. In the simulation, the following parameters are used: system AC voltage RMS value = 70 V, capacitor DC voltage $V_{dc} = 100$ V, $k = 10\%$, $V_{\max} = 15$ V. In Fig. 9 there are obviously three periods of capacitor voltage variation which correspond to three steps of the control strategies mentioned in Tables 2 and 3. Figure 10 shows the source current compensation result where the DC voltage imbalance is controlled simultaneously. However, as compared with Fig. 7, the current after compensation will be influenced. This is mainly due to the fact that when the DC voltage variation is larger than the maximum limitation $V_{\max}$, the switching time is dedicated to control the DC imbalance, not to the power quality compensation according to the control strategy in Table 3.

In simulation, the extreme case is chosen in order to explain the DC voltage variation control strategy more clearly. All the control strategies mentioned in Tables 2 and 3 are tested. As the triple harmonic components dominate the waveform of the neutral current in distribution site from statistical results, the strategy mentioned in Table 2 is enough for DC voltage variation control in most practical applications. In addition, the situation discussed in Table 3 can also be avoided by increasing the size of the DC capacitor so that better power quality compensating performance is obtained.

5 Experimental results

A two-level three-leg centre-split inverter prototype has been implemented. 3DSVM control strategy with DC variation control is achieved with 2.5 KHz switching frequency by a TMS320F2407 DSP controller. In the experiment the AC source voltage RMS value is 57 V and the DC voltage before compensation is controlled to 110 V. The value of the DC side capacitor is 10 mF.

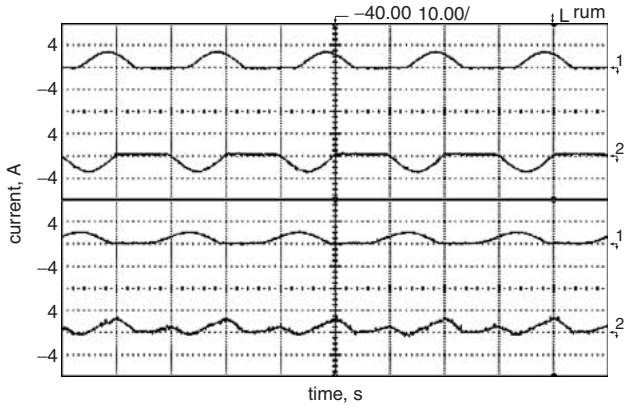

Fig. 11 *Current before compensation*

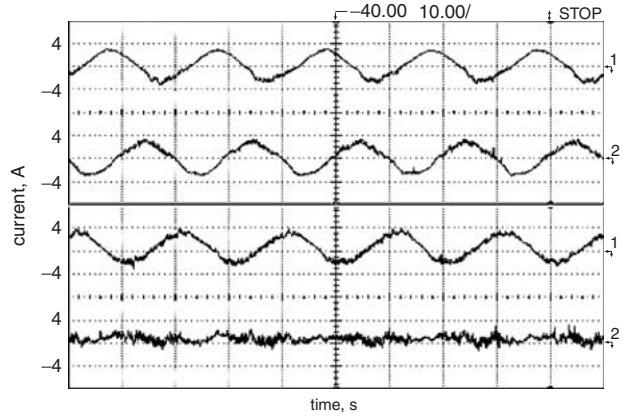

Fig. 12 *Current after compensation*

The load current recorded is shown in Fig. 11 before compensation. Figure 12 shows the source current after compensation. Current harmonics and neutral current are all compensated. Figures 13 and 14 show the DC voltage variation without and with dc imbalance control, respectively. The validity of 3DSVM and the DC voltage imbalance control strategy are proved.

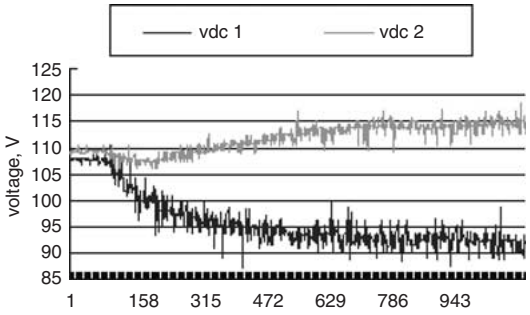

Fig. 13 *DC voltage without any control*

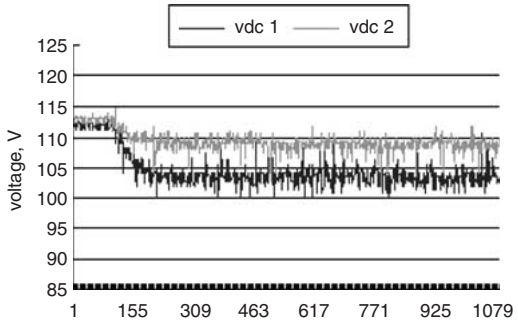

Fig. 14 *DC voltage after being controlled*

6 Conclusion

In this paper, a control technique named 3DSVM (three dimensional space vector modulation) for a two-level three-leg centre-split inverter is proposed with the DC voltage variation control strategy. Different from the conventional 2DSVM, there are eight different vectors corresponding to the eight switching states in 3DSVM instead of seven different vectors as in conventional two-level three-leg inverters. All eight vectors will contribute to the zero-sequence or neutral current compensation in the three-phase four-wire system. Unfortunately, there is no net-zero state in the two-level three-leg centre-split system, which can be chosen in redundant time. Therefore, the approximated progress is taken to estimate the product, which should be zero, of the net-zero vector and redundant time. The DC voltage variation which affects the origin or reference point along with the zero-axis can be controlled by varying the dwell-time of the zero vectors. The important outcome of this paper is that the larger voltage variation margin will have a better compensation performance in three-leg centre-split inverters. Fortunately, in practical electric distribution sites, the third harmonic component dominates the waveform of the neutral current. Hence, the possibilities of the current through the two DC-linked capacitors are almost the same, and voltage on one capacitor cannot continue to increase. In addition, increase in the capacity of the capacitor can increase the maximum limitation of DC voltage imbalance. Thus, the extreme case discussed in Section 4 can also be avoided Simulation and experimental results prove that, by using the 3DSVM control technique with DC voltage control, the current harmonics and neutral current can be compensated simultaneously, and the DC voltage variation can also be controlled.

7 Acknowledgment

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