An Analytical Linearization Method for CMOS MMIC Power Amplifier Using Multiple Gated Transistors

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Abstract: In this paper, a novel analytical linearization method for CMOS MMIC power amplifier based on parallel connection of transistors (also named Multiple Gated Transistors) is proposed. By this method, the power amplifier's IMD3 can be eliminated analytically by operating these transistors within the determined $g_m^*$ linearized range. In order to demonstrate the proposed method usefulness, a 900 MHz Class AB power amplifier using 4 NMOS transistors with maximum aspect ratio (W/L)=1300/0.5 is designed based on 0.35 μm CMOS process. The simulated results demonstrate that -76dB IMD3 can be obtained with 13dB as power gain.

I. Introduction

The linearity of the MMIC power amplifier is of paramount importance for modern narrow band mobile communication system. Unlike the wide-band applications, unwanted harmonics may be easily filtered out. In the narrow-band application, harmonic non-linearity is of main concern. In particular, IMD3 (3rd Intermodulation Distortion) presents serious interference problem as this IMD3 appears in the pass-band with other legitimate signal and this unwanted IMD3 is not easily be filtered out [1]. In order to tackle this IMD3, there are many techniques reported in the past few years [2-4]. Most of them rely on additional complex circuit to achieve MMIC power amplifier linearization. According to the topological similarities, there are three main techniques [5-7].

- Feedback
- Feedforward
- Predistortion

In order to reduce the circuitry complexity as addressed in the above approaches, a FET-level IMD3 linearization method using multiple-gated transistors is proposed even there is little insight of the analytical design [8]. As such, an analytical linearization method for this multiple-gated transistors linearization is presented in this paper with the special emphasis on the IMD3 and gain.

Besides this introduction, section II of this paper presents the analytical method for the power amplifier linearization technique using multiple-gated transistors whilst some simulation results based on 0.35μm CMOS process will be presented in section III in order to illustrate linearized power amplifier performance. Finally, the conclusion will be drawn in section IV.

II. Analytically Linearization Method

In this section, an analytical linearization technique is proposed based on the multiple-gated transistors approach [8]. By the Taylor series, the drain current $i_{ds}$ of a MOSFET is related to the gate-source voltage and drain source voltage, it can be described as follows:

$$i_{ds}(v_{gs}) = i_{dc} + g_m v_{gs} + g_m^2 v_{gs}^2 + g_m^3 v_{gs}^3 + ...$$  (1)

where $g_m$ represents the transconductance of the MOSFET. From Eq. (1), it is obvious that IMD3 will be directly related to $v_{gs}^3$. As such, its coefficient plays a important role to the power amplifier linearization. Two conventional MOSFETs' $g_m^*$ subject to different bias conditions is plotted in Fig. 1. Both of them show one positive peak and one negative peak as depicted in Fig. 1.
It can be noticed that most of the MOSFET based amplifiers will be biased at saturation region as the situation of MOSFET. Therefore, amplifier’s IMD将会 be mainly resulted from the negative peak of $g_m^*$. The reduction of this negative peak from maximum value to zero intuitively implies the IMD3 elimination. In order to achieve this IMD3 reduction, an auxiliary MOSFET2 is arranged in parallel with MOSFET1 and a Class AB power amplifier circuitry based on this parallel multiple-gated transistors is constructed and shown in Fig. 2(a) and Fig. 2(b) respectively. According to the proposed approach, the dash-block in Fig. 2(b) is replaced by the multiple-gated transistors configuration in Fig. 2(a). The negative peak of the MOSFET1’s $g_m^*$ can be cancelled by the MOSFET2’s $g_m^*$ positive peak value subject to different bias points as shown in Fig. 3. Moreover, a linearized range of the composite $g_m^*$ as depicted in Fig. 3 is resulted and so IMD3 can be significantly reduced if the amplifier is operated in this range.

The key analysis issue is then the analytical determination of the above linearized range. In fact, the bias voltage $V_{GS2}$ of MOSFET2 should be chosen as follows:

$$V_{GS2} = V_{GS1} - \Delta V_{GS}$$

(2)

![Fig. 1 DC characteristics of 2 MOSFETs](image1)

Fig. 1 DC characteristics of 2 MOSFETs

![Fig. 2 (a) Multiple-Gated Transistors Linearization Configuration](image2)

Fig. 2 (a) Multiple-Gated Transistors Linearization Configuration

In addition, the positive peak of MOSFET1 could be located at a value of $V_{GS1} = x_1$ such that

$$\frac{\partial g_m^*}{\partial v_{GS1}}|_{v_{GS1}=x_1} = 0 \text{ and } \frac{\partial^2 g_m^*}{\partial v_{GS1}^2}|_{v_{GS1}=x_1} < 0$$

(3)

As such, there are two values of $V_{GS1}$ satisfying the above criteria, denoted as $g_m^*(x_1)$, one in the cutoff region and one slightly greater than $V_{GS1}$. The one in the cutoff region is ignored because the MOSFET1 will not be biased at this region in general.

Similarly, the negative peak determination is as follows:

$$\frac{\partial g_m^*}{\partial v_{GS1}}|_{v_{GS1}=x_2} = 0 \text{ and } \frac{\partial^2 g_m^*}{\partial v_{GS1}^2}|_{v_{GS1}=x_2} > 0$$

(4)

Also, there are two values of $V_{GS1}$ satisfying the above criteria, denoted as $g_m^*(x_2)$, one in subthreshold region and this is always ignored. Then, the suitable region is saturation ones.

Therefore, the required linear range is determined by

$$\Delta V_{GS} = |x_1 - x_2|$$

(5)
It is also true that multiple MOSFETs connected in parallel will increase this linear region as shown in Fig. 4.

III. Simulation Results

To verify the above, four power amplifiers using multiple-gated transistors linearization method are simulated based on conventional 0.35μm CMOS technology [9-10]. The MOSFET1 is biased at VGS1 and the other transistors are biased evenly from VGS1 respectively. This implies that MOSFET2 is biased at VGS1-0.14V and so forth. The bias point of MOSFET1 is at the center of the linearized region. The gate lengths of different MOSFETs are all 0.5 μm, and the widths are 1300μm, 650μm, 500μm, and 420μm respectively. All of the bias differences and the sizes are determined according to the above analysis. The RF performance of the amplifier are tested by applying two-tone signals input of 900 and 905MHz with input power of -15 dBm and the supply voltage of 4V.

From Fig. 5, it is obvious that power amplifier with 4 MOSFETs can obtain superior IMD3 (about -76dB) and power gain as high as 13dB subject to VGS1 = 0.75V. As such, this confirms the usefulness of the power amplifier using multiple-gated transistor linearization method.

IV. Conclusion

An analytical linearization method for MMIC power amplifier is presented in this paper. The required linearized range for the $g_m$ is derived and illustrated by 4 power amplifiers. It is reported that power amplifier with 4 MOSFETs connected as multiple-gated structure offers IMD3 as good as -76dB and power gain as high as 13dB.

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Reference